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BOMOPTION	P72 OASIS GOOD	P72 OASIS BETTER	P73 OASIS BEST	P72 MIRAGE GOOD	P72 MIRAGE BETTER	P73 MIRAGE BEST
DD1X	X	X	X	X	X	X
DD2X						
600MHZ	X			X		
700MHZ		X	X		X	X
OASIS	X	X	X			
MIRAGE				X	X	X
MID OR HIGH RANGE NO PWRSTEP	X	X	X	X	X	X
HIGH_PLL_RANGE_NO_PWRSTEP						
MID OR HIGH RANGE PWRSTEP						
HIGH PLL PANGE PWRSTEP						
LOW PLL RANGE						
LOW OR MID PLL RANGE	X	X	X	X	X	X
FIREWIRE	X	X	X	X	X	X
NO FIREWIRE						
PWRSTEP						
NO PWRSTEP	X	X	X	X	X	X
100MHZ	X	X	X	X	X	X
66MHZ						
3SBAT	X	X		X	X	
4SBAT			X			X
SWCHG						
HWCHG	X	X	X	X	X	X
OASIS_600	X					
OASIS_700		X	X			
MIRAGE_600				X		
MIRAGE_700					X	X
INTUSB	X	X	X	X	X	X
NON PRODUCTION						
SLOW_CHRG	X	X		X	X	
FAST_CHRG			X			X
128M	X	X	X	X	X	X
256M						
TBEN						

P72/73 (JUN 04 /2002)

PAGE 1 : COVER PAGE (CONTENTS)

PAGE 2 : BLOCK DIAGRAM

PAGE 3 : PROCESSOR

PAGE 4 : CPU PLL CONFIGURATION

PAGE 5 : PANGEA PROCESSOR I/F

PAGE 6 : PANGEA SDRAM & SO-DIMMS I/F & SS CLK GEN

PAGE 7 : SDRAM ON-BOARD BANKS

PAGE 8 : SO-DIMM CONNECTOR

PAGE 9 : PANGEA AGP IF

PAGE 10 : PANGEA ETHERNET, FIREWIRE, PWR/GNDS

PAGE 11 : PANGEA BYPASS

PAGE 12 : PANGEA ATA, & I/O BUS

PAGE 13 : PANGEA SER/AUD/USB, BOOTSTRAPS

PAGE 14 : PULL-UP/PULL-DOWN (1)

PAGE 15 : PULL-UP/PULL-DOWN (2)

PAGE 16 : MODEM & HD/CD-ROM CONNECTORS

PAGE 17 : USB PORT

PAGE 18 : 10/100M ETHERNET PHY

PAGE 19 : FIREWIRE PHYSICAL LOGIC

PAGE 20 : CARDSLOT (WIRELESS) INTERFACE & BOOTROM

PAGE 21 : PMU (POWER MANAGEMENT UNIT)

PAGE 22 : GRAPHICS CONTROLLER

PAGE 23 : GRAPHICS CONTROLLER POWER

PAGE 24 : LCD I/F

PAGE 25 : VIDEO CONNECTOR

PAGE 26 : IRDA/BT USB CONNECTOR

PAGE 27 : SNAPPER,CONTROL & D/A

PAGE 28 : SNAPPER AUDIO, HEADPHONE DRIVER

PAGE 29 : SNAPPER AUDIO, MICROPHONE PREAMP

PAGE 30 : POWER SYSTEM ARCHITECTURE

PAGE 31 : DC POWER JACK

PAGE 32 : BATTERY CHARGER

PAGE 33 : BATTERY INTERFACE

PAGE 34 : POWER SUPPLY 3V/5V MAIN SWITCHERS

PAGE 35 : POWER SUPPLY LOAD FET SWITCHES

PAGE 36 : CORE SWITCHERS & SUPER CAP CIRCUIT

PAGE 37 : ATI_CORE AND 2.5V_MAIN SWITCHERS

PAGE 38 : CPU_VCORE(1.2/1.4V) SWITCHERS

PAGE 39 : TOOLING HOLES

PAGE 40 : CONSTRAINTS -- POWER

PAGE 41 : CONSTRAINTS -- CPU BUS

PAGE 42 : CONSTRAINTS -- MEMORY BUS (1)

PAGE 43 : CONSTRAINTS -- MEMORY BUS (2)

PAGE 44 : CONSTRAINTS -- AGP & FIREWIRE

PAGE 45 : CONSTRAINTS -- MISCELLANEOUS

PAGE 46 : NET ATTRIBUTES

PAGE 47 : REVISION HISTORY (1)

PAGE 48 : REVISION HISTORY (2)

PAGE 49 : REFERENCE DESIGNATOR LOCATION INDEX (1)

PAGE 50 : REFERENCE DESIGNATOR LOCATION INDEX (2)

PAGE 51 : REFERENCE DESIGNATOR LOCATION INDEX (3)

PAGE 52 : REFERENCE DESIGNATOR LOCATION INDEX (4)

PAGE 53 : REFERENCE DESIGNATOR LOCATION INDEX (5)

P. LEADER	APPROVED BY	CHECKED BY	PREPARED BY

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PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
REV	1.C	1.0	1.B	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.B	1.B	1.0	1.0	1.0	1.C	1.0	1.0	1.0	1.0	1.0	1.0	1.0
DATE	0604	0312	0522	0312	0312	0312	0312	0312	0312	0312	0312	0312	0312	0522	0522	0312	0312	0312	0604	0312	0312	0312	0312	0312	0312	0312
27	28	29	30	31	32	33	34	35	36	37	38	39	39	41	42	43	44	45	46	47	48	49	50	51	52	53
1.0	1.B	1.0	1.0	1.0	1.0	1.A	1.0	1.B	1.0	1.0	1.B	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.C	1.0	1.0	1.0	1.0	
0312	0502	0312	0312	0312	0312	0402	0312	0522	0312	0312	0522	0312	0312	0312	0312	0312	0312	0312	0312	0312	0604	0312	0312	0312	0312	

P/N:820-1320

RFA # 222273

ATC P/N:KK0U22701110U02

ATC DRAWING NO.: U227-1-3-08

COVER PAGE (CONTENTS)

DESCRIPTION:

iBook MLB & SCHEMATIC

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ACI:C

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53

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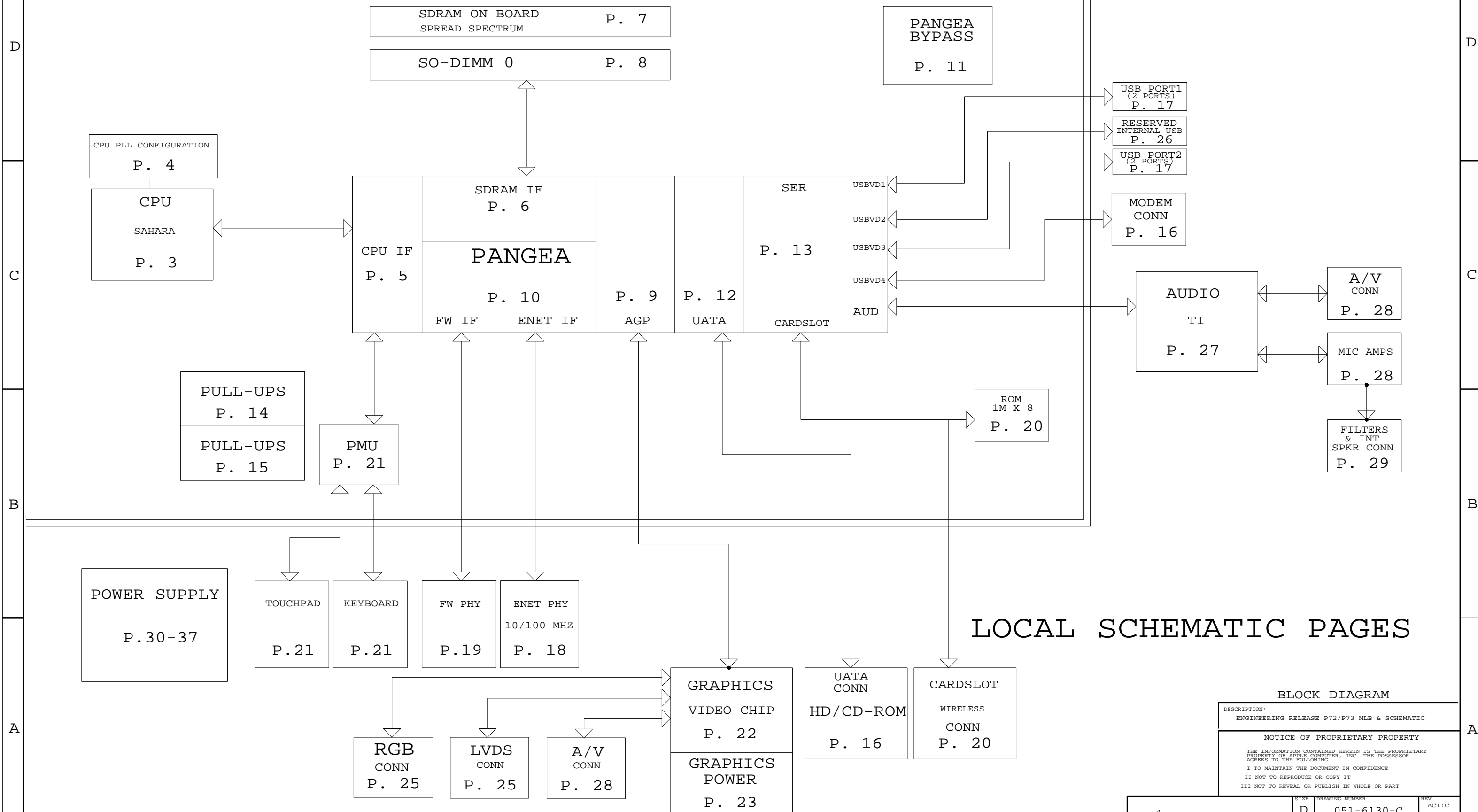
3

2

1

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CORE SCHEMATIC PAGES



LOCAL SCHEMATIC PAGES

BLOCK DIAGRAM

DESCRIPTION:

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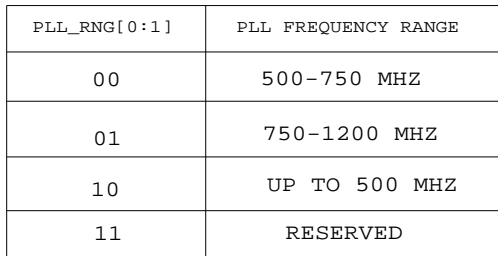
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BUS SPEED		66	100
CPU_PLL_CFG[0:4]	CORE:BUS RATIO		
00000	OFF		
00001	OFF		
00010	PLL BYPASS		
00011	PLL BYPASS		
00100	2.0:1	N/A	N/A
00101	2.5:1	N/A	N/A
00110	3.0:1	N/A	N/A
00111	3.5:1	N/A	N/A
01000	4.0:1	N/A	N/A
01001	4.5:1	N/A	N/A
01010	5.0:1	N/A	500
01011	5.5:1	N/A	550
01100	6.0:1	N/A	600
01101	6.5:1	N/A	650
01110	7.0:1	N/A	700
01111	7.5:1	500	750
10000	8.0:1	533	800
10001	8.5:1	567	850
10010	9.0:1	600	900
10011	9.5:1	633	950
10100	10.0:1	667	1000
10101	11.0:1	733	N/A
10110	12.0:1	800	N/A
10111	13.0:1	867	N/A
11000	14.0:1	933	N/A
11001	15.0:1	1000	N/A
11010	16.0:1	N/A	N/A
11011	17.0:1	N/A	N/A
11100	18.0:1	N/A	N/A
11101	19.0:1	N/A	N/A
11110	20.0:1	N/A	N/A
11111	OFF		



14A7 14A6 13D1 5C2 4D5 3D5 3C4 46B7
36B4 35C3 15D2 15B1 14D8 14D6 14C6

+VIO_CPU_SLEEP

LOW PLL RANGE

R853
4.7K
5%
1/16W
MF
2 603

3A6 PLL_RNG<0>

MID OR HIGH RANGE PWRSTEP

Q806
2N7002
3M

MID OR HIGH RANGE NO PWRSTEP

R1122
10K
5%
1/16W
MF
2 603

3A6 PLL_RNG<1>

HIGH PLL RANGE PWRSTEP

Q807
2N7002
3M

HIGH_PLL_RANGE_NO_PWRSTEP


R1123
4.7K
5%
1/16W
MF
2 603

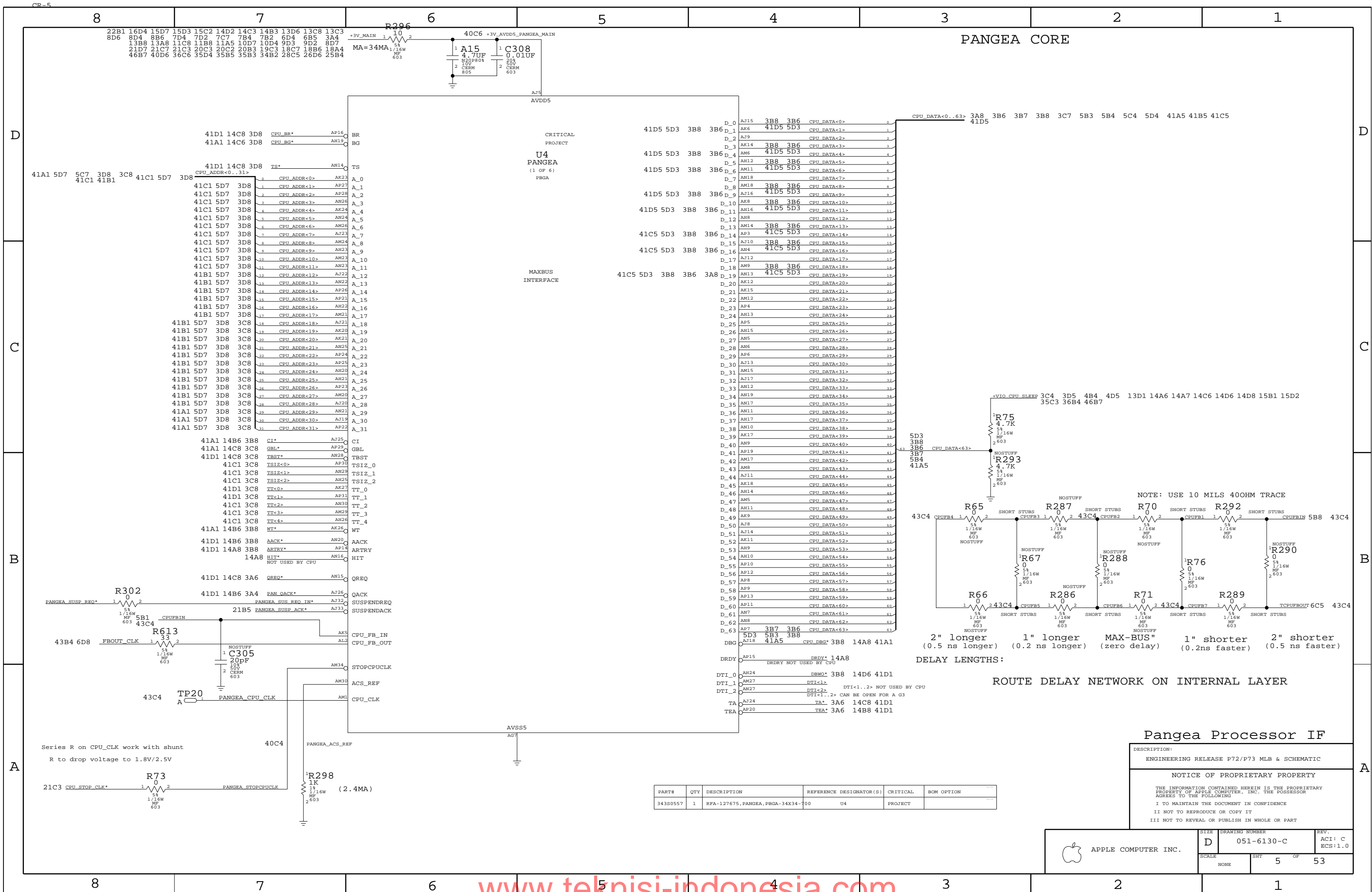
LOW OR MID PLL RANGE

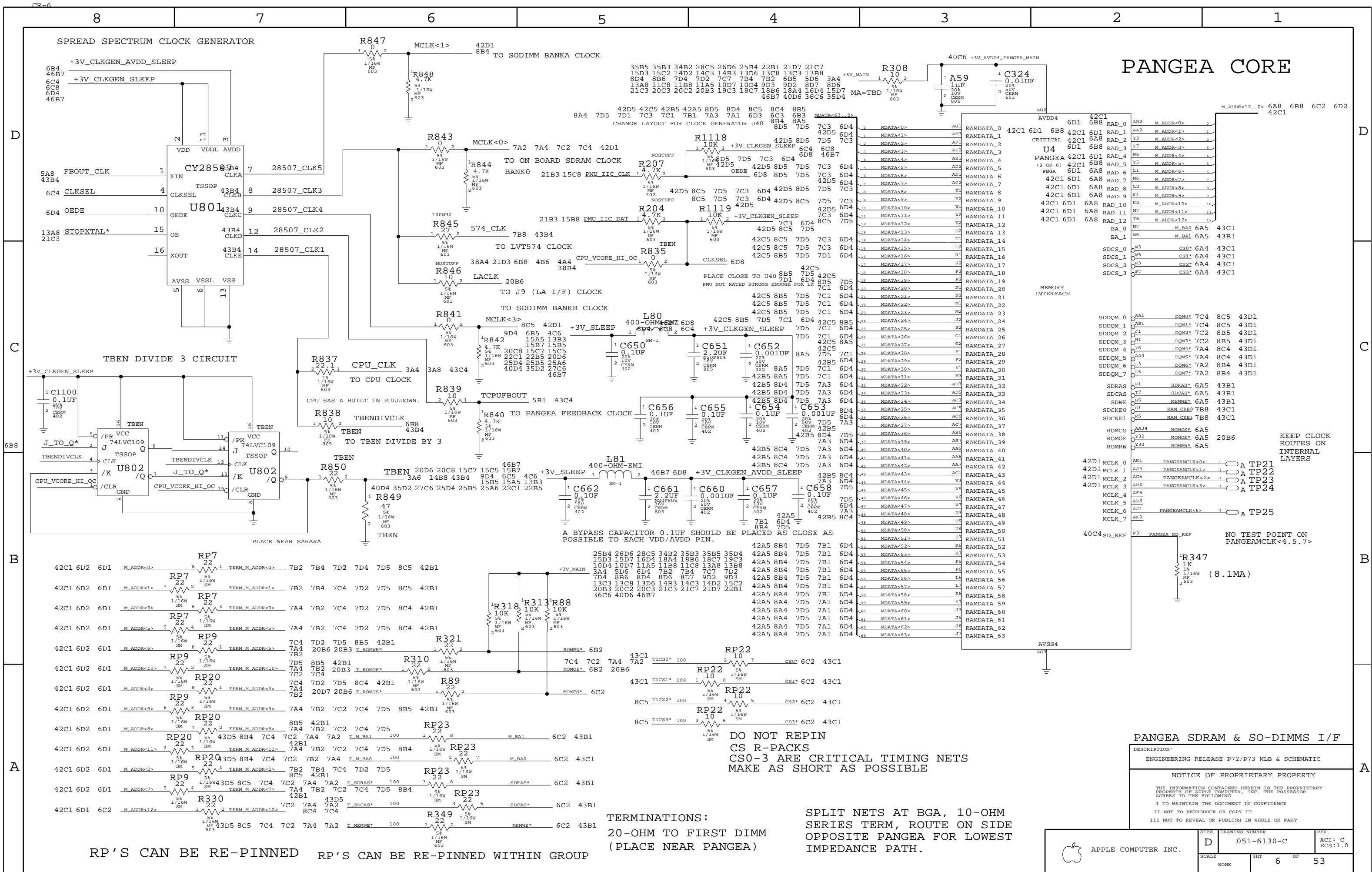
R831
10K
5%
1/16W
MF
2 603

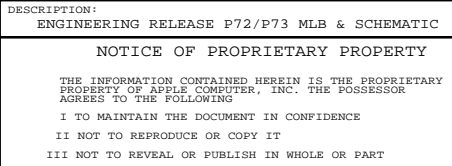
3A4 21D3 6C5 6B8 4B6 CPU_VCORE_HI_OC

0:1]

 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6130-C	REV. ACI: c ECS:1.0
	SCALE NONE	SHT 4	OF 53

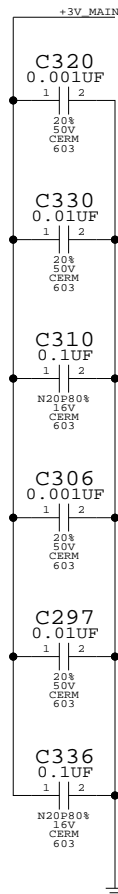




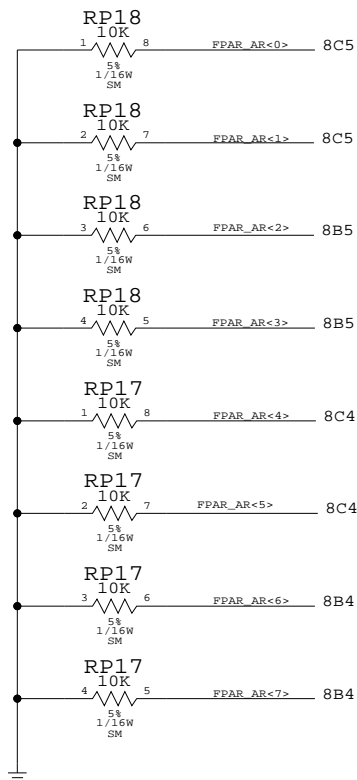


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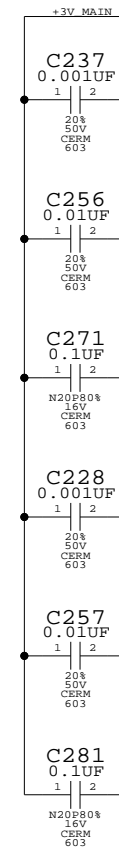
20C2 20C3 21C3 21C7 21D7 22B1 25B4 26D6 28C5 34B2 35B3
11B8 11C8 13A8 13B8 13C3 13C8 13D6 14B3 14C3 14D2 15C2 15D3 15D7 16D4 18A4 18B6 18C7
3A4 5D6 6B5 6D4 7B2 7B4 7C7 7D2 7D4 8B6 8D4 8D7
8B6 8D4 8D6 9D2 9D3 10D4 10D7 11A5 11B8 11C8 13A8 13B8 13C3 13C8
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35B5 35D4 36C6 40D6 46B7



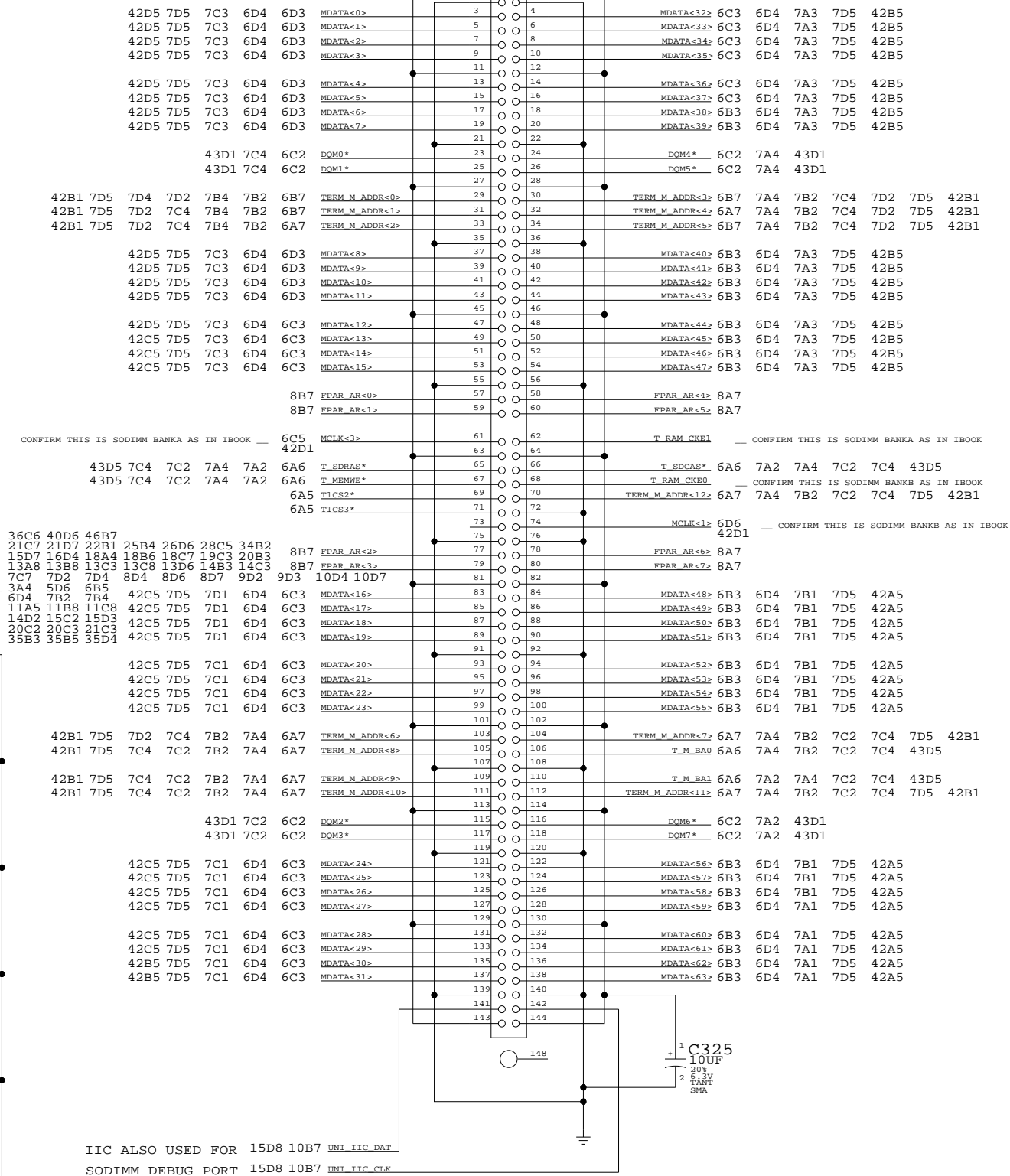
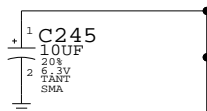
PULL-DOWN UNUSED PARITY BITS



RP'S CAN BE RE-PINED
OR TURNED INTO DISCRETES
BY PCB DESIGNS.

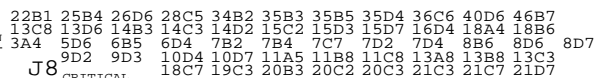


34B2 35B3 35B5 35D4 36C6 40D6 46B7
13D6 14B3 14C3 14D2 15C2 15D3 15D7 16D4 18A4 18B6 18C7
3A4 5D6 6B5 6D4 7B2 7B4 7C7 7D2 7D4 8B6 8D4 8D7
9D2 9D3 10D4 10D7 11A5 11B8 11C8 13A8 13B8 13C3 13C8
19C3 20B3 20C2 20C3 21C3 21C7 21D7 22B1 25B4 26D6 28C5



IIC ALSO USED FOR 15D8 10B7 UNI_IIC_DAT
SODIMM DEBUG PORT 15D8 10B7 UNI_IIC_CLK

PUT EACH 10UF CAP AT EACH END
AND HIGH-SPEED BYPASS DISTRIBUTED
ALONG SODIMM



SO-DIMM CONNECTOR

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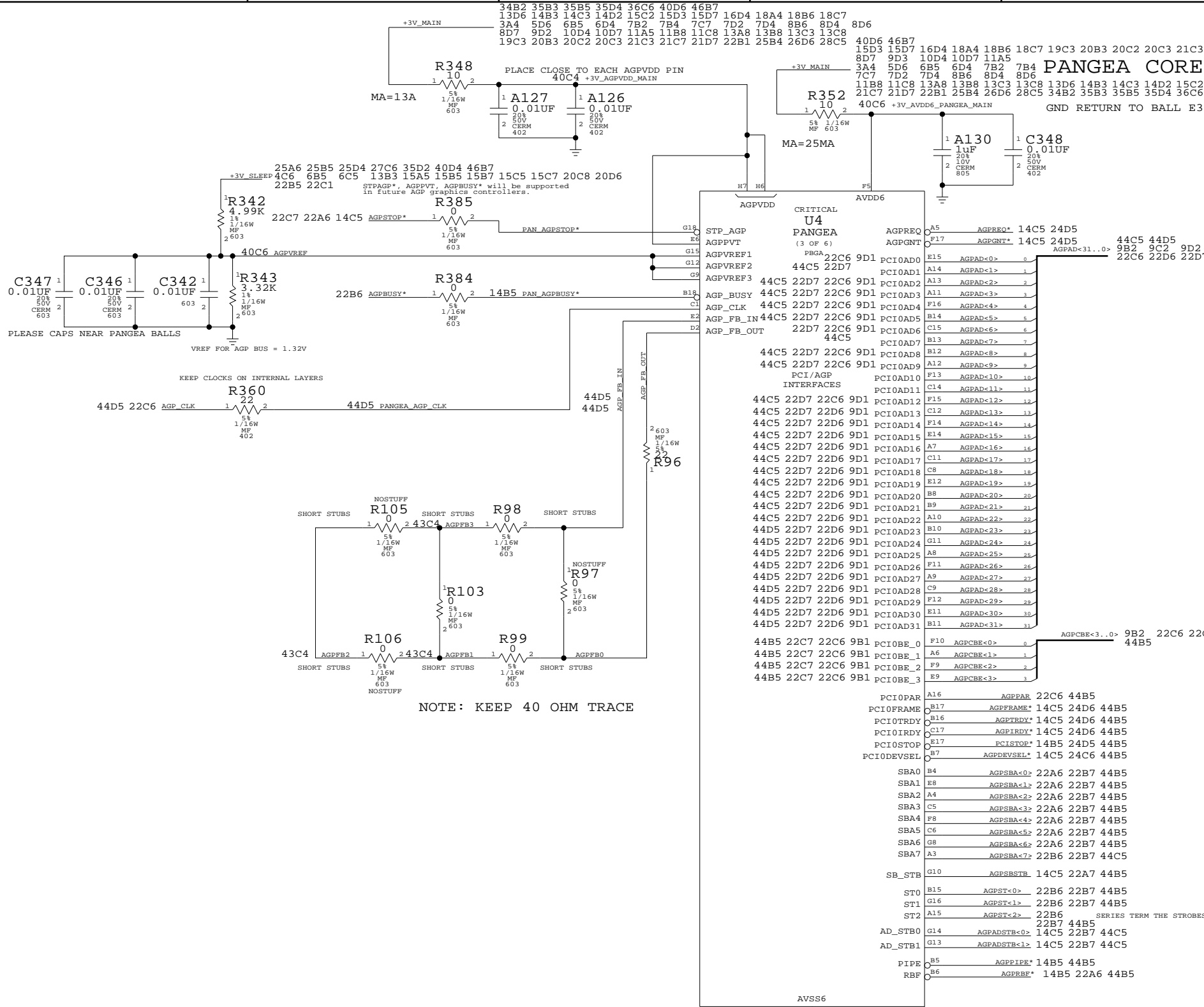
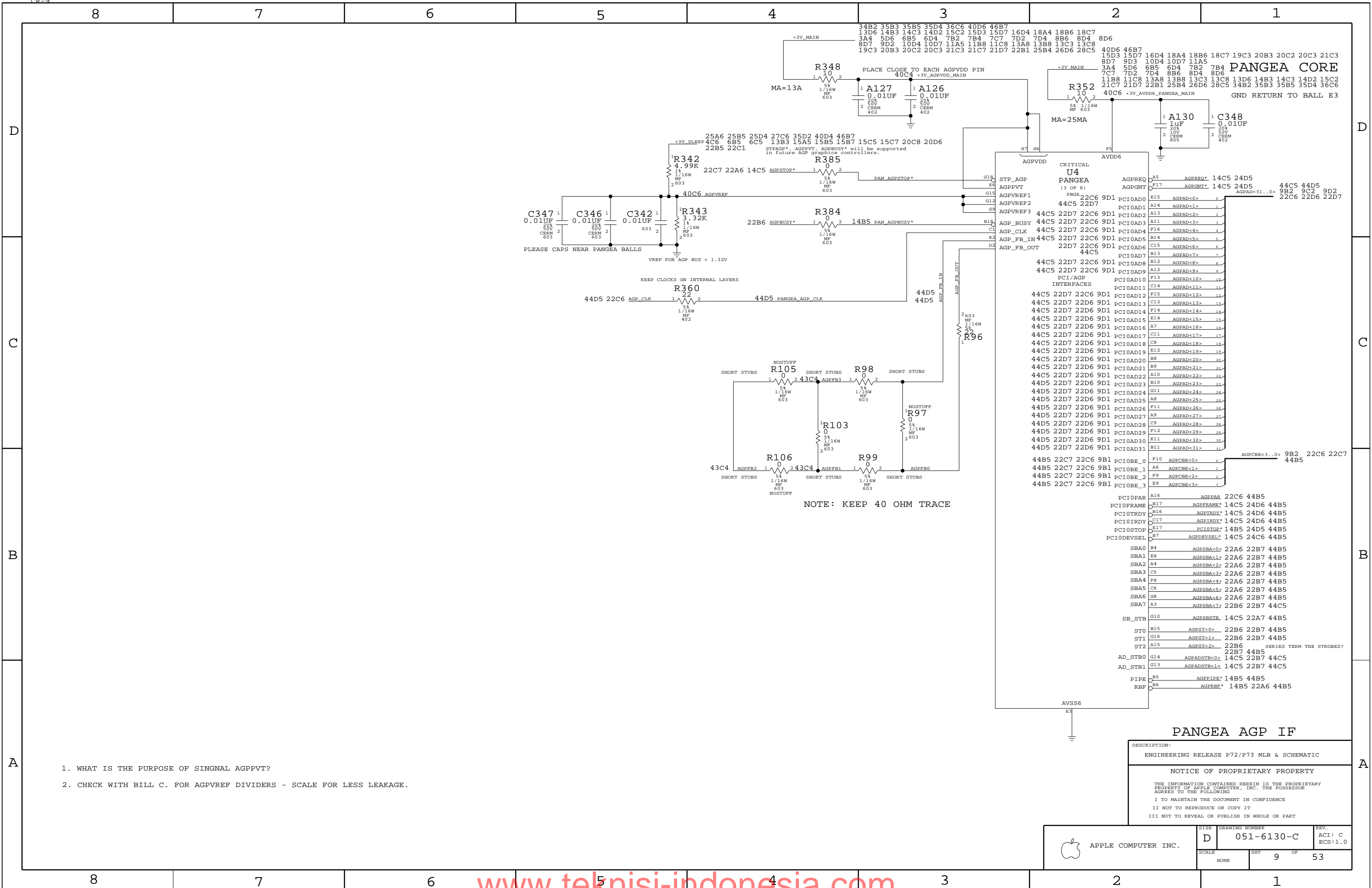
OF

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REV.

ACI: C

ECS:1.0



PANGEA AGP IF

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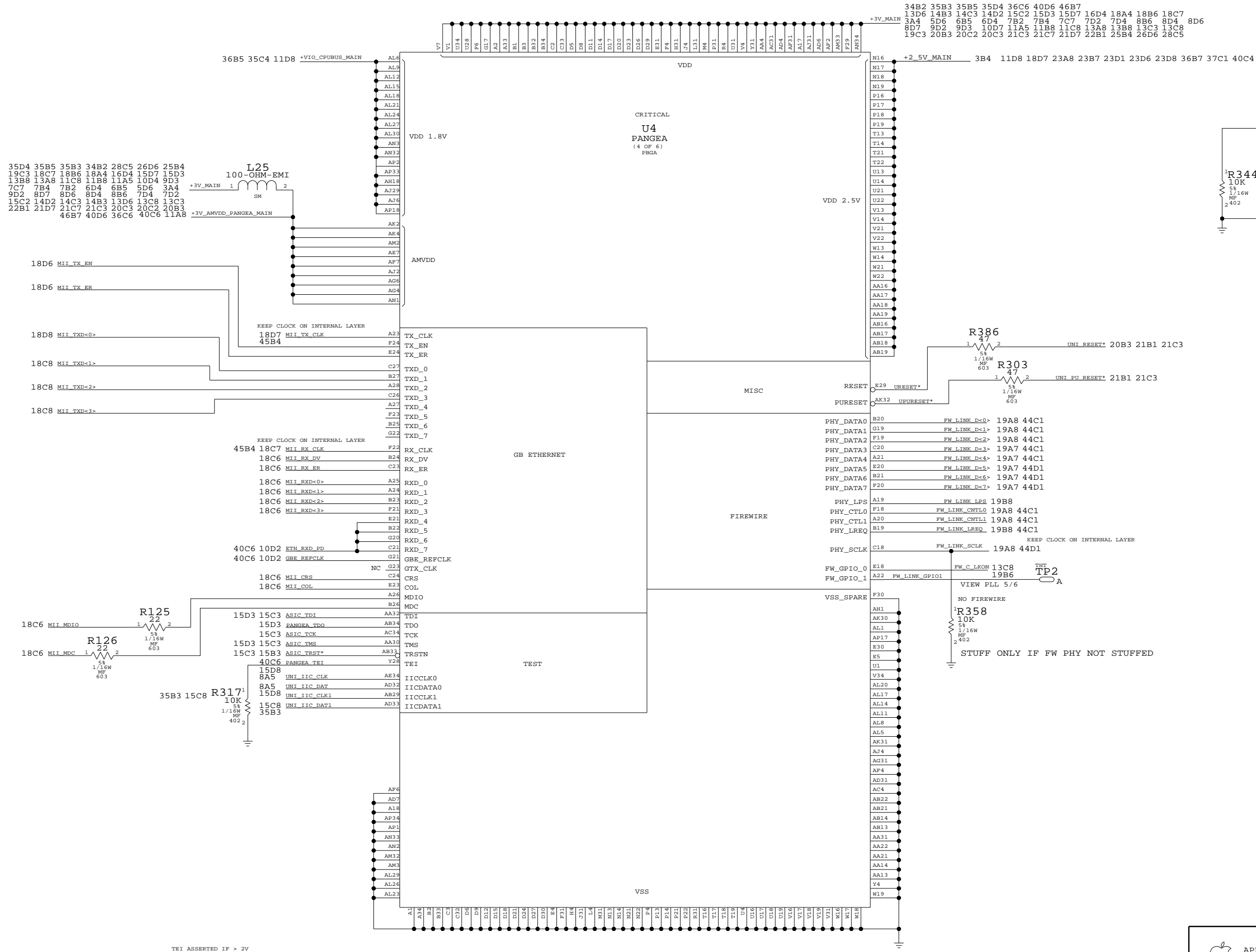
D

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B

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PANGEA CORE



TEI ASSERTED IF > 2V

Pangea Ethernet, Firewire, Pwr/GNDs

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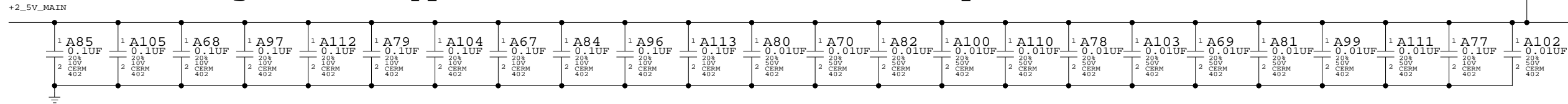


APPLE COMPUTER INC.

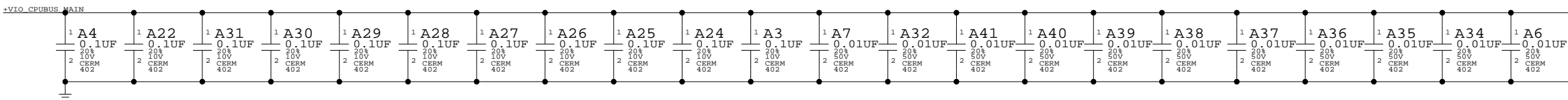
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SCALE	SHT	10 OF 53
NONE		

PANGEA CORE

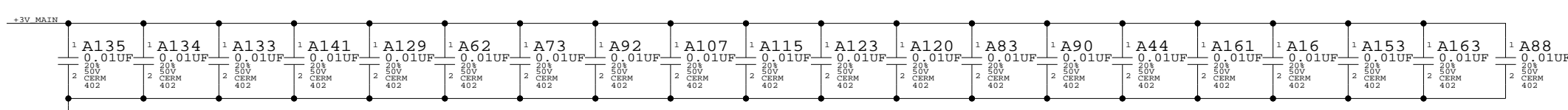
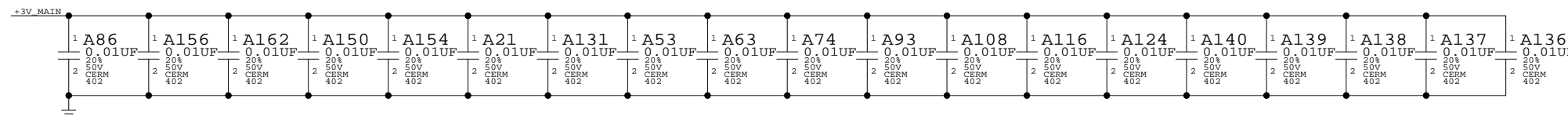
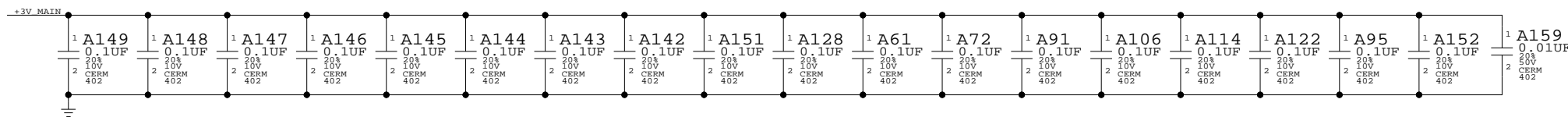
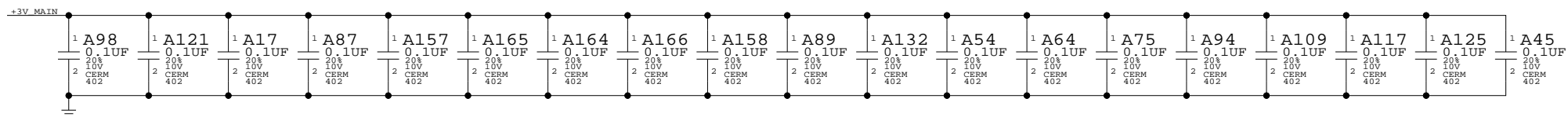
Pangea Core Bypass -- 16 0.01uF across each pair, 8 0.001uF on corners



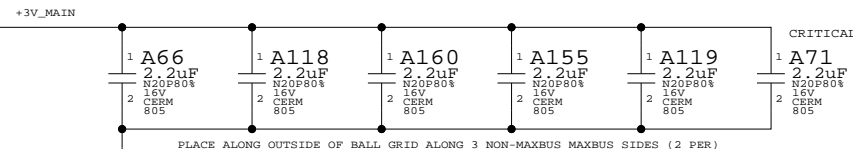
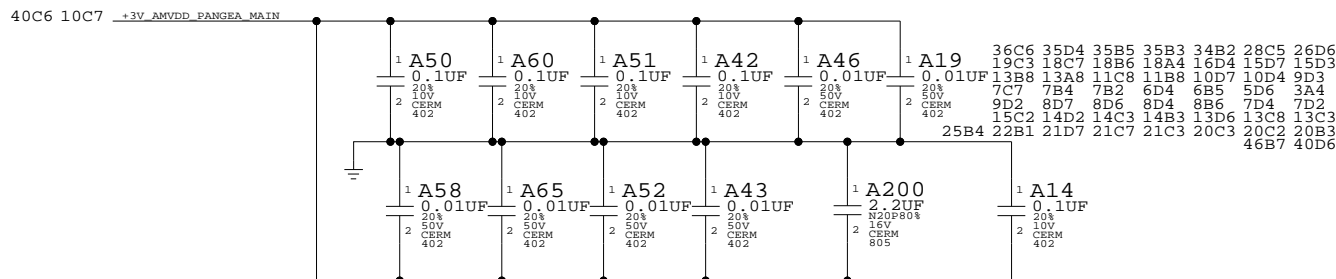
Pangea Processor I/F Bypass -- two per power/ground pair



Pangea I/O Ring Bypass -- two per power/ground pair



Pangea AMVDD Bypass (one pair per pin)



Pangea Bypass

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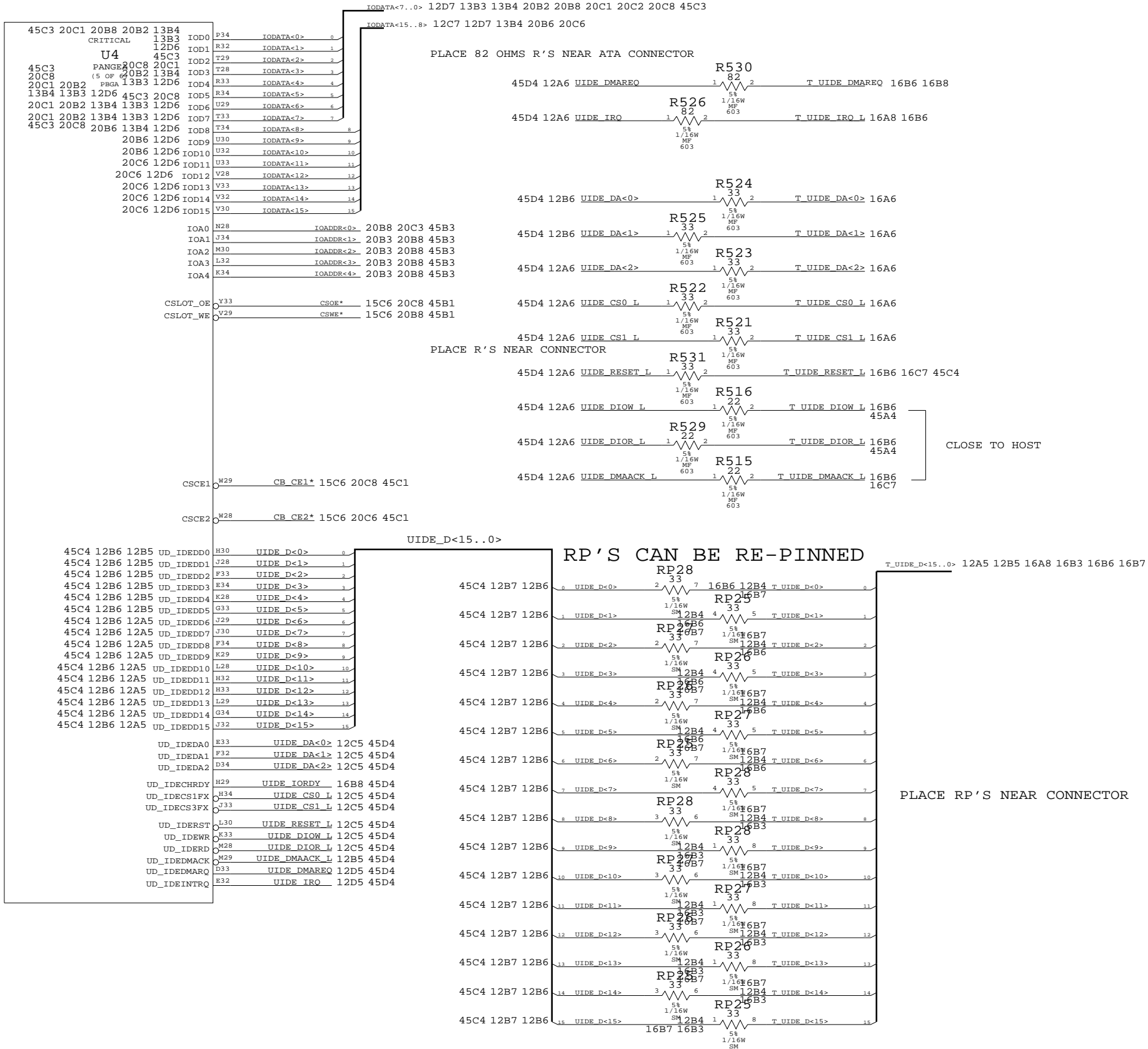
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SCALE	SHT	OF
NONE	11	53

PANGEA CORE



PANGEA ATA BUS

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SCALE	SHT	OF
NONE	12	53

PANGEA CORE

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D

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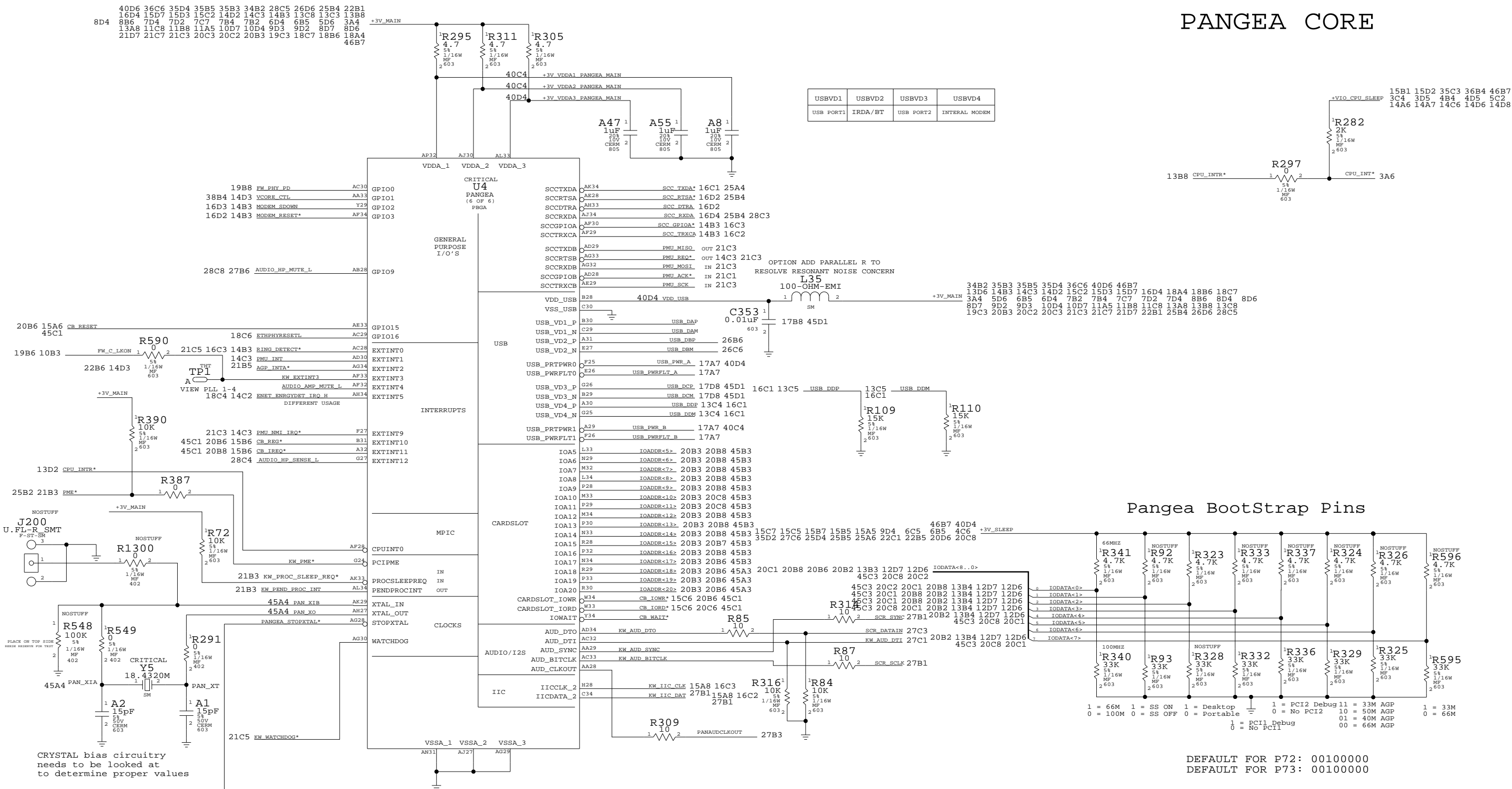
C

B

B

A

A



DEFAULT FOR P72: 00100000
DEFAULT FOR P73: 00100000

PANGEA SER/AUD/USB, BOOTSTRAPS

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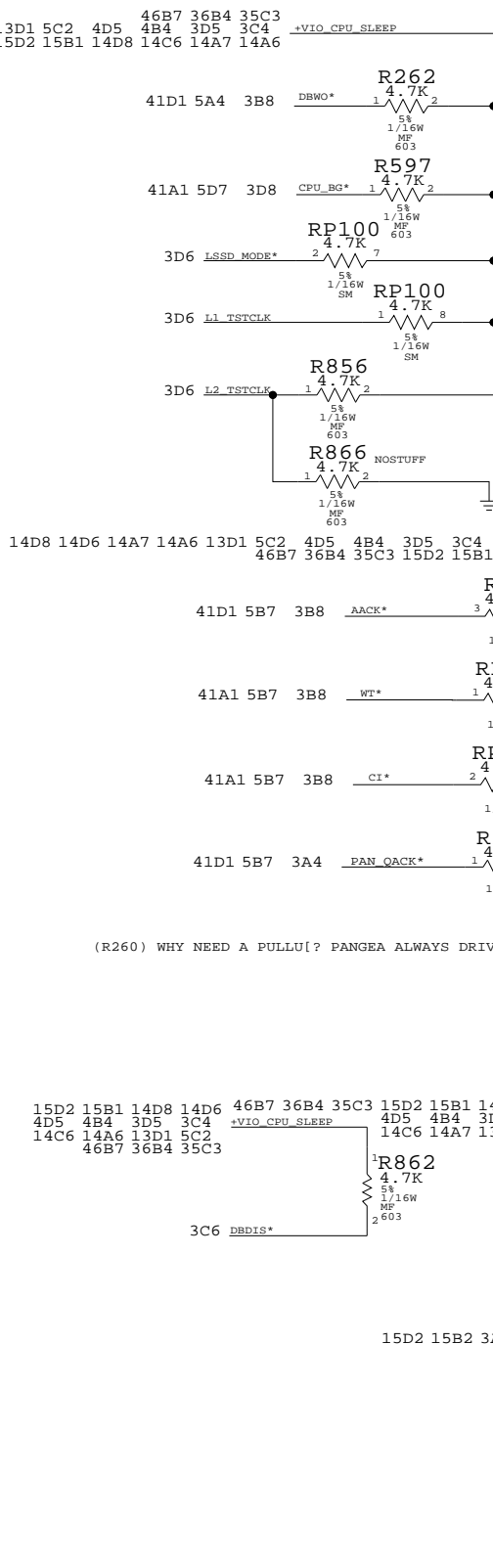
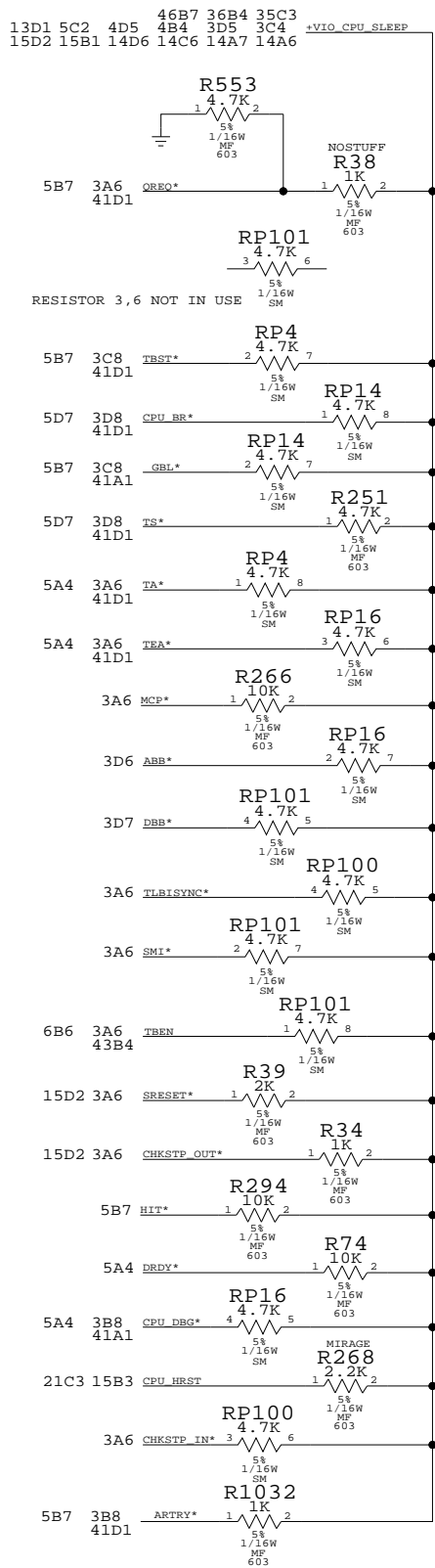
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	D	051-6130-C	
NONE		13	53

PANGEA PULLUPS/PULLDOWNS

TO LOCATE UNUSED RPAK PINS REFERE TO COMPONENT LOCATIO CREF TABLE ON PAGE 49

MAXBUS PULLS



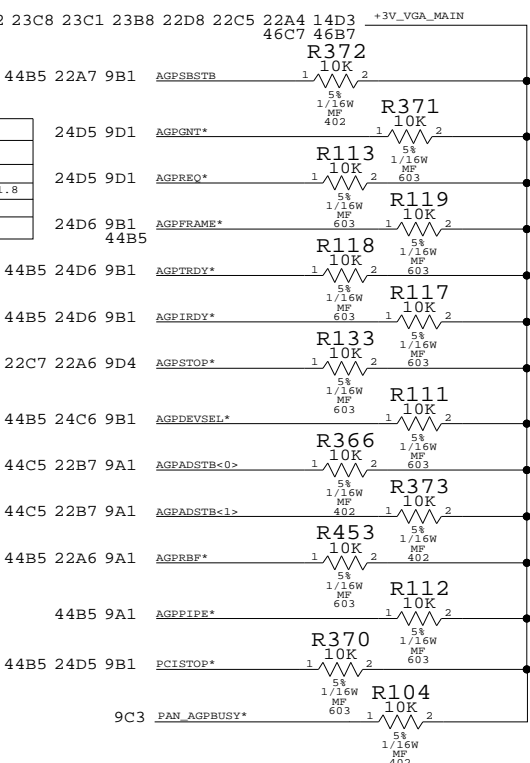
SAHARA V2.0		
BVSEL	L1_TSTCLK	I/O VOLTAGE
B'0'	B'0'	N/A
B'0'	B'1'	1.2, 1.5, OR 1.8
B'1'	B'0'	3.3
B'1'	B'1'	2.5

NOTE:

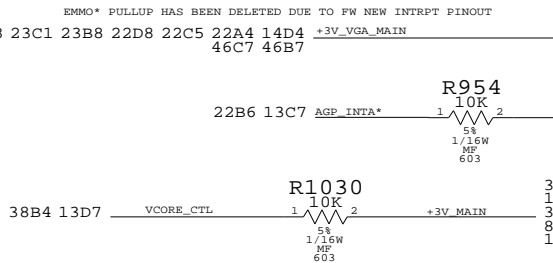
FOR SAHARA V1.1, L1_TSTCLK

MUST BE TIED TO A LOGICAL '1'

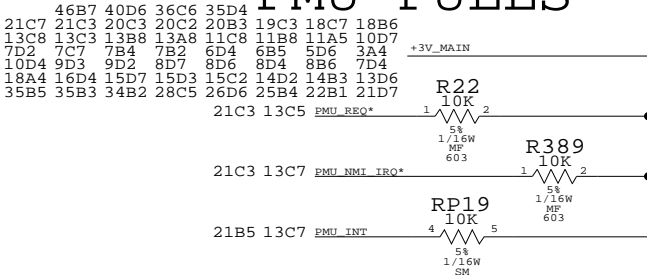
AGP PULLS



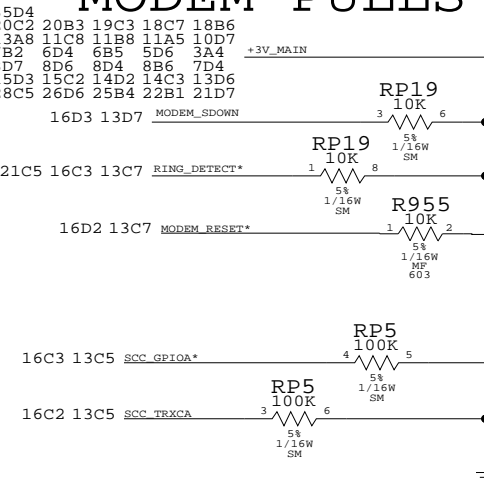
GPIO PULLS



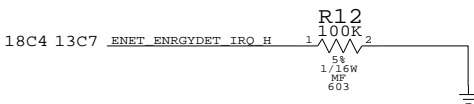
PMU PULLS



MODEM PULLS



ENET PULLS



NEW 4.7K RESISTORS CAN BE
CHANGED INTO R-PACKS

R-PACKS CAN BE RE-PINNED

PULL-UP/PULL-DOWN (1)

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

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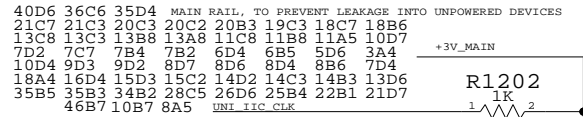
SCALE NONE SHEET 14 OF 53

TO LOCATE UNUSED RPAK PINS REFERE TO COMPONENT LOCATIO CREF TABLLE ON PAGE49

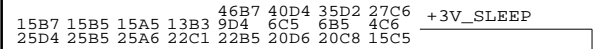
IIC BUS PULLUPS

CARDSLOT BUS PULLS

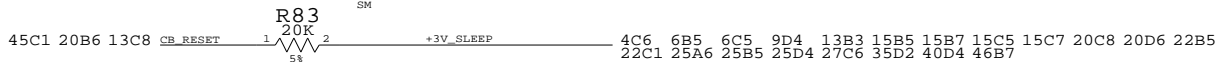
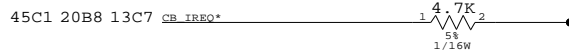
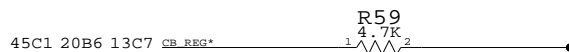
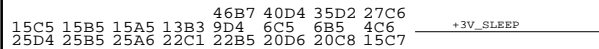
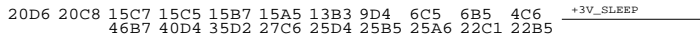
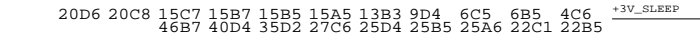
JTAG PULLS



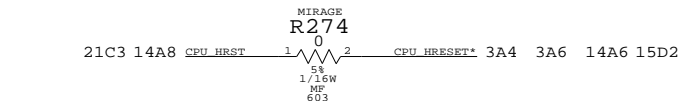
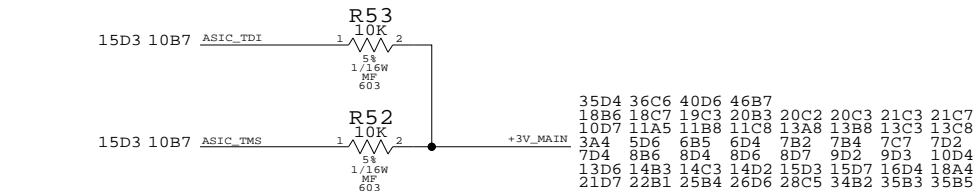
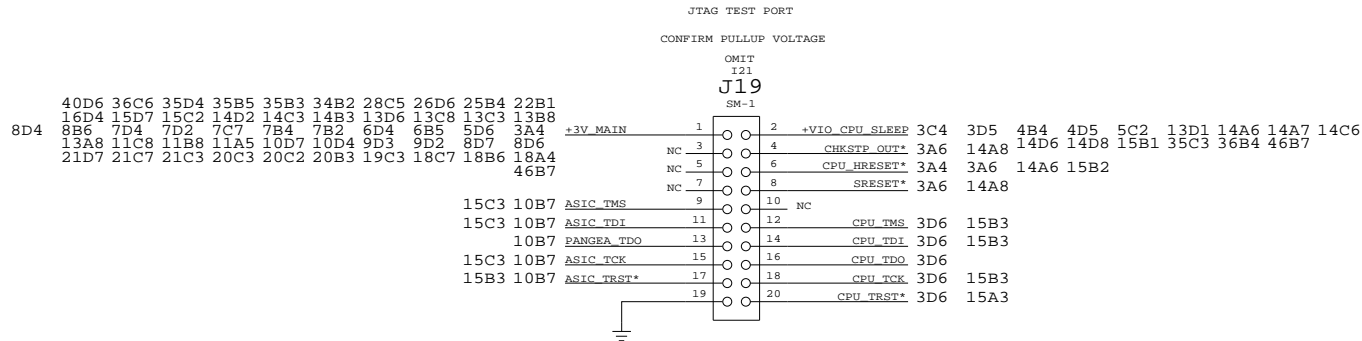
PMU NOT RATED STRONG ENOUGH FOR 1K



PMU PULL UP



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
630-3999	1	PCBA, BOOTBANGER, P72	J19	OASIS
511S0018	1	CONN, POPT, STR 20-P .8MM PITCH	J19	NONPRODUCTION



PULL-UP/PULL DOWN(2)

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC


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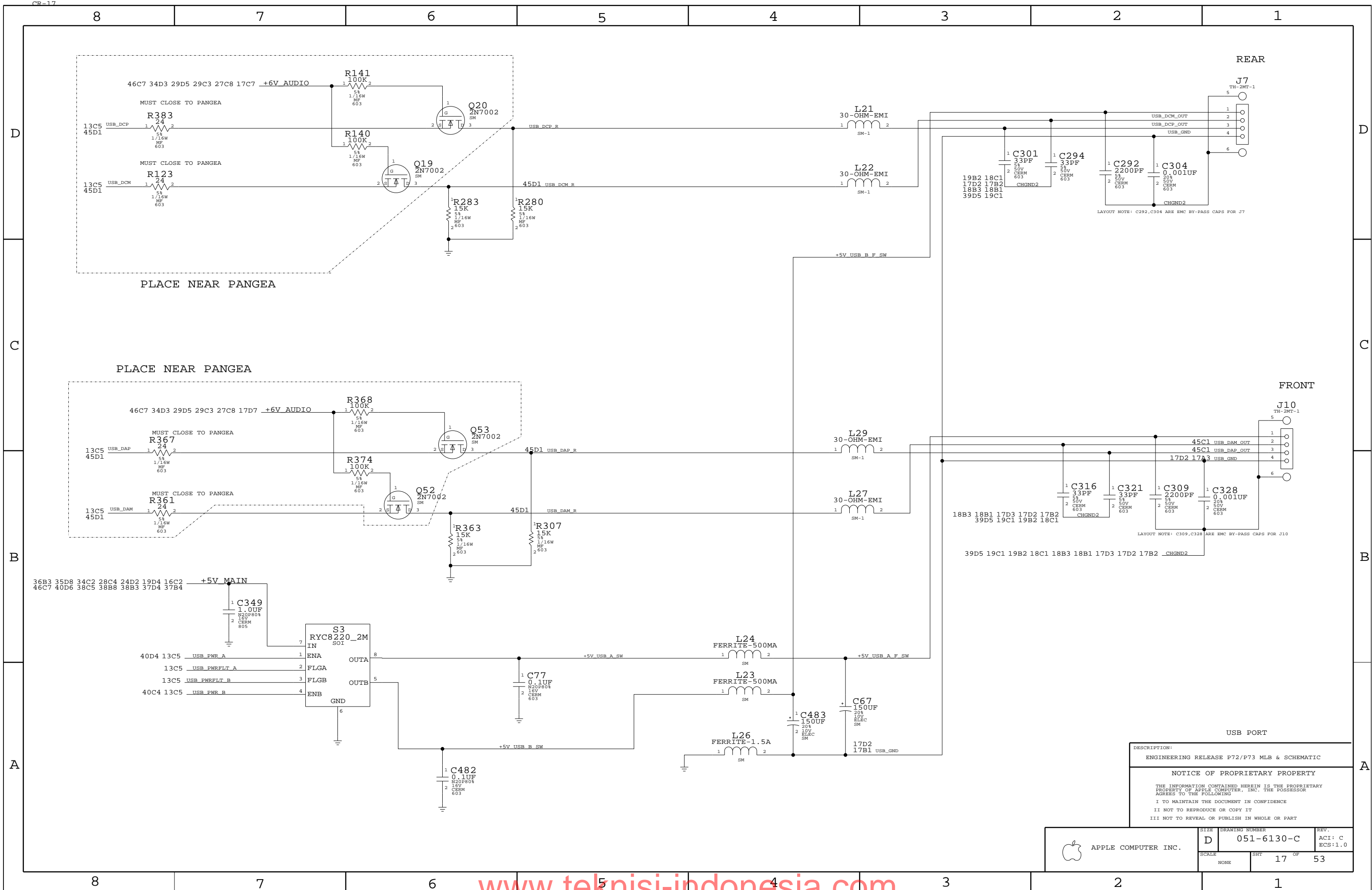
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D	051-6130-C	ACI: C ECS:1.B
SCALE	SHT	OF
NONE	15	53

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	SCALE	SMT	OF	
	NONE	16	53	



40C4 37C1 36B7 23D8 23D6 23D1 23B7 23A8 11D8 10D3 3B4 +2_5V_MAIN 1 L2 FERRITE-500MA 2 +2_5V_ENET_MAIN 18B4 18B7 18C3 18C4 18D3

C17 10UF 20% 10V TANT SMR

PLACE R4, R7, C18 CLOSE TO THE PHY

PLACE R191 AND R192 CLOSE TO PHY

10C8 MII_TXD<0> 1 33 2 R195 5% 1/16W MP 603

10C8 MII_TXD<1> 1 33 2 R197 5% 1/16W MP 603

10C8 MII_TXD<2> 1 33 2 R201 5% 1/16W MP 603

10C8 MII_TXD<3> 1 33 2 R205 5% 1/16W MP 603

TXD(N), NEED BUS CONSTRAINTS ADDED SO 33 OHMS ARE CLOSE TO PANGEA.

34B2 28C5 26D6 25B4 22B1 21D7 21C7 21C3 20C3 14D2 14C3 14B3 13D6 13C8 13C3 13B8 13A8 11C8 7D4 7D2 7C7 7B4 7B2 6D4 6B5 5D6 3A4 11B8 11A5 10D7 10D4 9D3 9D2 8D7 8D6 8D4 20C2 20B3 19C3 18B6 18A4 16D4 15D7 15D3 15C2 46B7 40D6 36C6 35D4 35B5 35B3

+3V_MAIN 18B8 18A6 MII_PWR_EN_L 10B8 MII_MDC 10B8 MII_MDIO 13C7 ETHPHYRESETL

18C6 18A6 MII_PWR_EN_L

Q36 2N7002

CRITICAL 25MHZ XTALI XTALOUT

18C6 18B8 MII_PWR_EN_L

Q7 2N7002

Q35 2N7002

31C5 31B5 AC_VOLT 1 470K 2 R198 5% 1/16W MP 603

C15 1UF 20% 10V CERM 805

C176 0.1UF 20% 10V CERM 603

18C6 18B8 MII_PWR_EN_L

18C6 18B8 MII_PWR_EN_L

18C6 18B8 MII_PWR_EN_L

18D3 18C4 18C3 18B7 18B4 18D6

18D3 18C4 18C3 18B7 18B4 18D6

18D3 18C4 18C3 18B7 18B4 18D6

18D3 18C4 18C3 18B7 18B4 18D6

18D3 18C4 18C3 18B7 18B4 18D6

18D3 18C4 18C3 18B7 18B4 18D6

18D3 18C4 18C3 18B7 18B4 18D6

18D3 18C4 18C3 18B7 18B4 18D6

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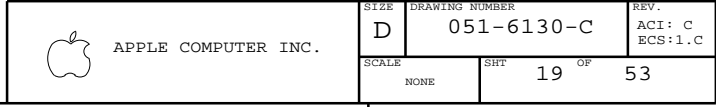
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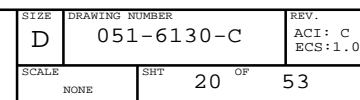
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18D3 18C4 18C3 18B7 18B4 18D6

18D3 18C4 18C3 18B7 18B4 18D6

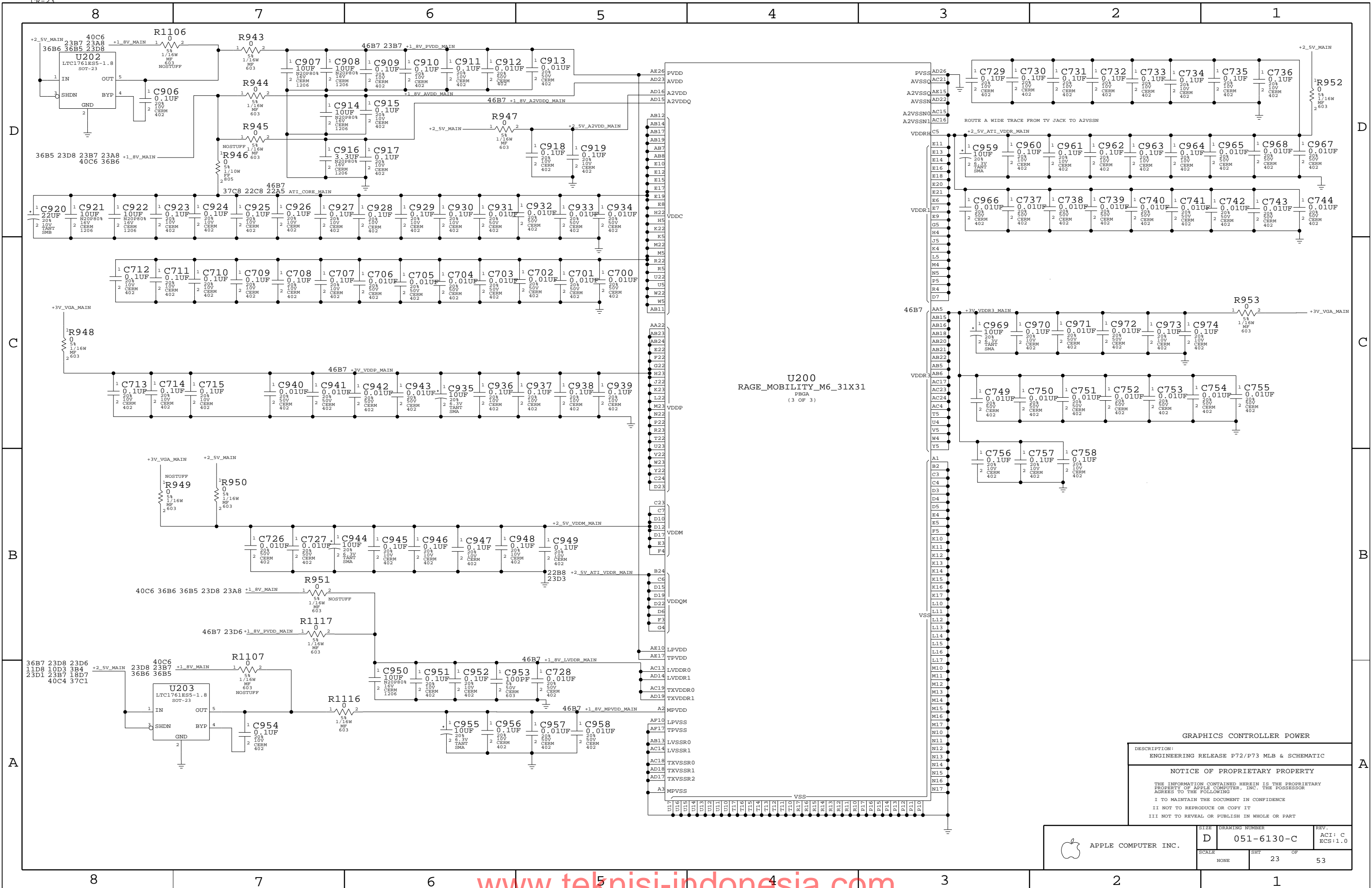
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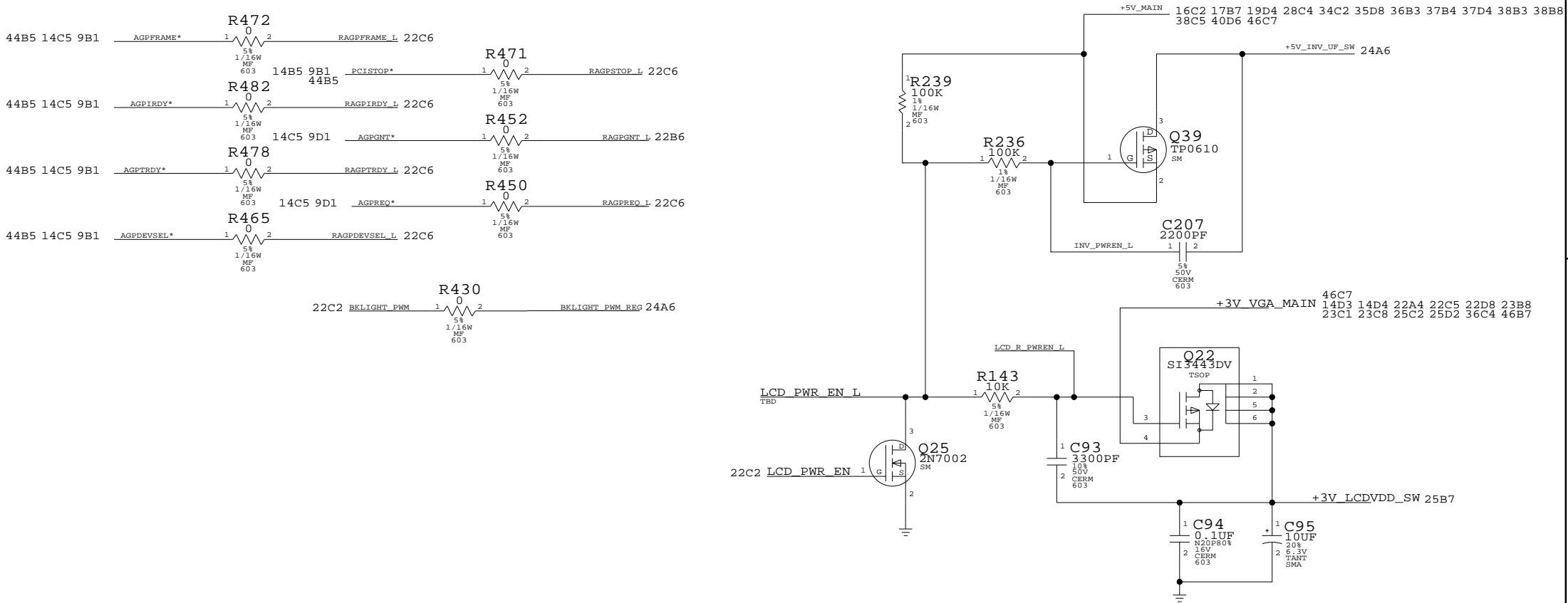




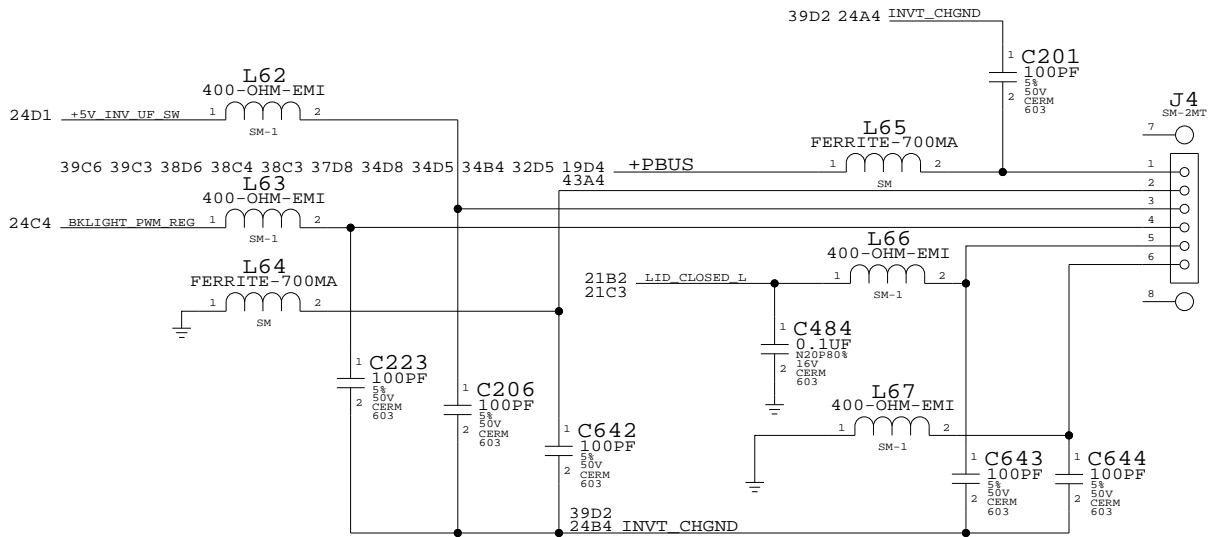




AGP BUS SERIES TERM



INVERTER CONNECTOR



EMC_GND DETERMINED BY ATC LAYOUT

LCD I/F

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

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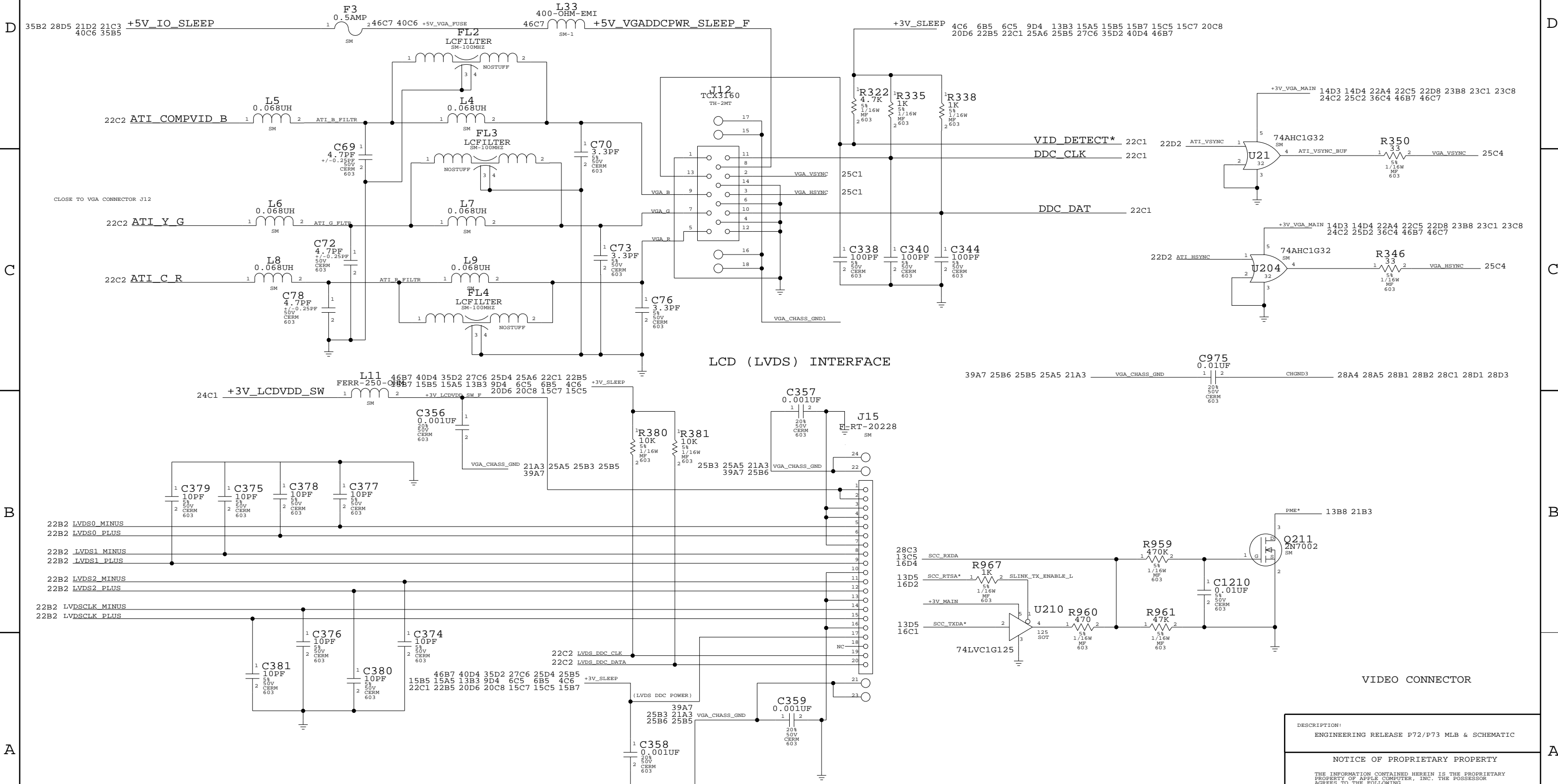
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D	051-6130-C	ACI: C ECS:1.0
SCALE	SHT	24 OF 53
NONE		

Video Connectors

EXTERNAL VIDEO (VGA) INTERFACE

NOTES :

DUE TO EMI CONCERNS,THE FOLLOWING PINS(WHICH ARE LOCATED OVER THE CORRECT PORTION OF THE VGA_CHASS_GND1 PLANE) ARE CONNECTED TO THE VGA_CHASS_GND1 PLANE AS WELL AS DIGITAL GROUND.....
R90-2, C69-2, C70-2, C76-2, FL2-3/4, FL4-3/4, J12-1/4/6/14, C338-2, C339-2, C340-2, C344-2,



DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

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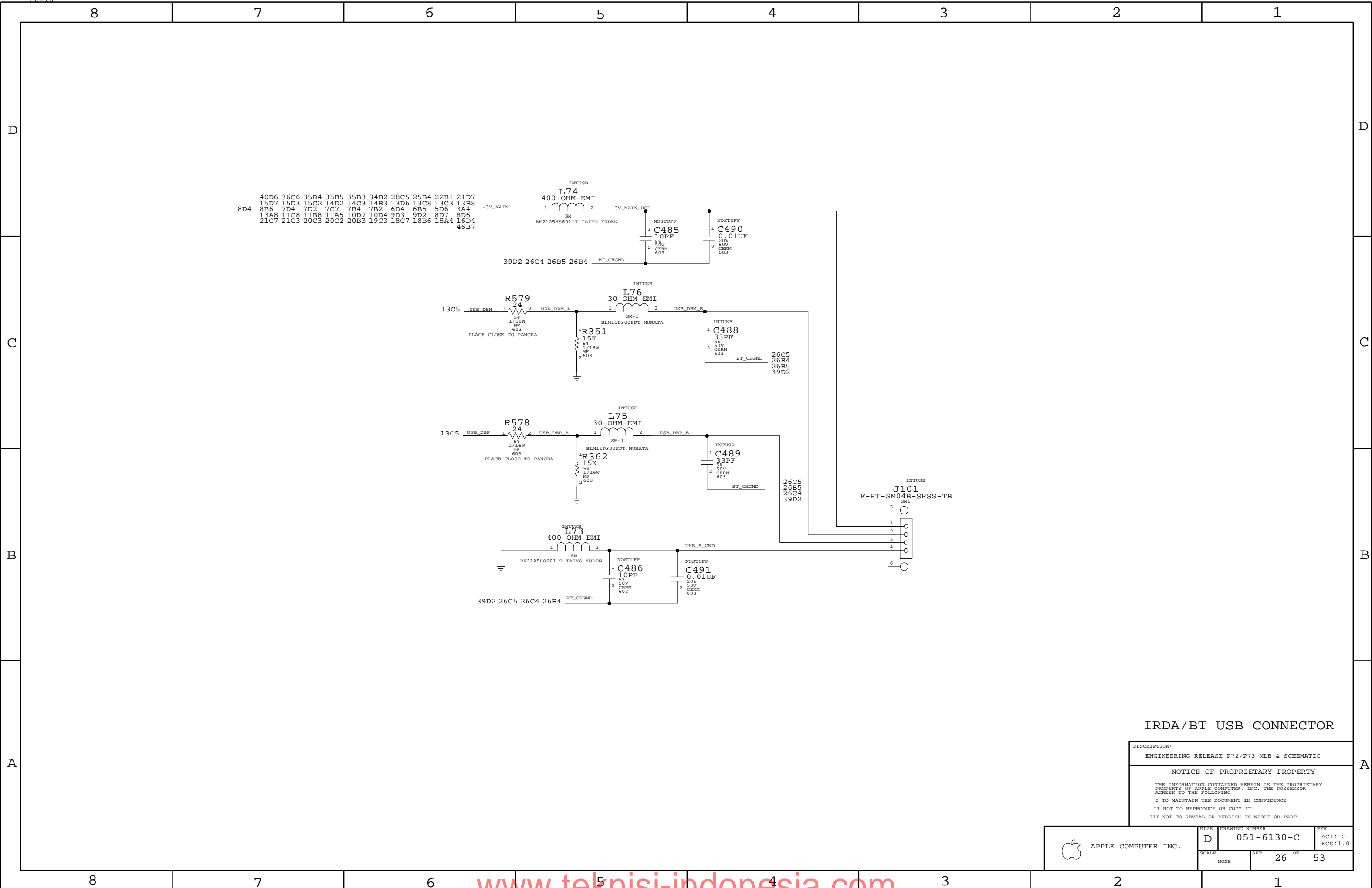
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SCALE	SHT	25	OF 53
NONE			



IRDA/BT USB CONNECTOR

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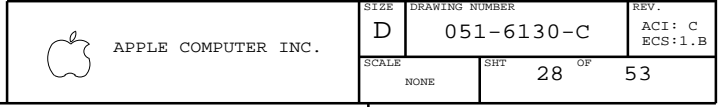
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6130-C	REV. ACI: C ECS:1.0
	SCALE NONE	SHT 26	OF 53



NONE	27	53
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D

D

C

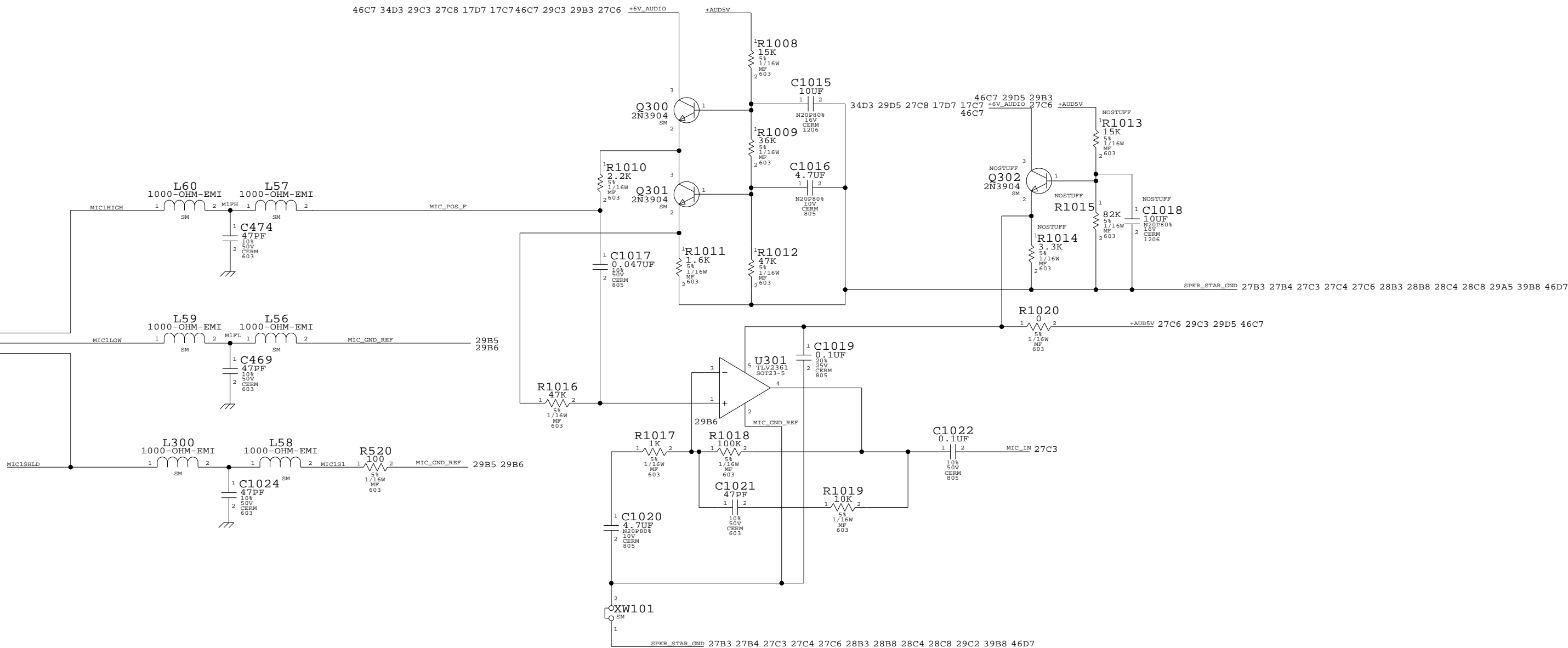
C

B

B

A

A



SNAPPER AUDIO, MICROPHONE PREAMP

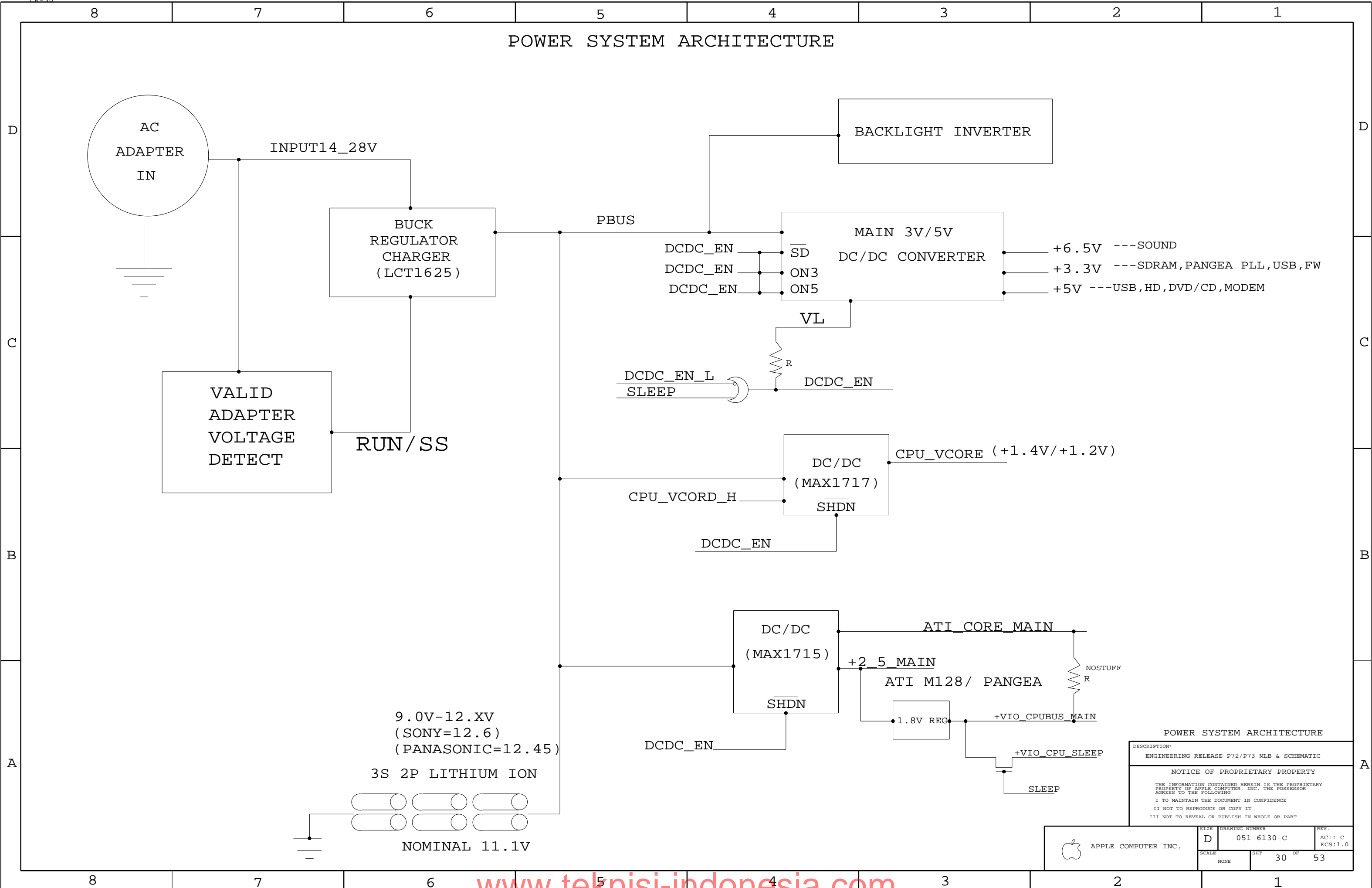
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE	SHT	29 OF 53
NONE		



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
110S2873	1	CHIP RES 1/16W 1% 2.87K 0603 ACI	R539	SLOW_CHRG
110S2613	1	CHIP RES 1/16W 1% 2.61K 0603 ACI	R539	FAST_CHRG

39C6 39C3 38D6 38C4 38C3 37D8 34D8 34D5 34B4 24A4 19D4 43A4 +PBUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
103S0568	1	CHIP RES 1/16W 1% 15.4K 0603 ACI	R495	3SBAT
103S0612	1	CHIP RES 1/16W 1% 11.3K 0603 ACI	R495	4SBAT
110S3012	1	CHIP RES 1/16W 1% 301 0603 ACI	R496	3SBAT
110S1502	1	CHIP RES 1/16W 1% 150 0603 ACI	R496	4SBAT

34C3 34C6 34D8 36C6 37A7 28B5 31C2 31C4 31D6 32A2 32A3 32D1 33A4 33A6 33B3 33B6 33B7 33C7 34A2 34B3 34B4 34C1 37B1 37B8 37C4 37D8 39A6 39B3

DESCRIPTION:
ENGINEERING RELEASE P72/73 MLB & SCHEMATIC

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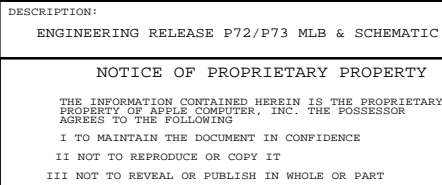
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SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE	SHT	OF
NONE	32	53

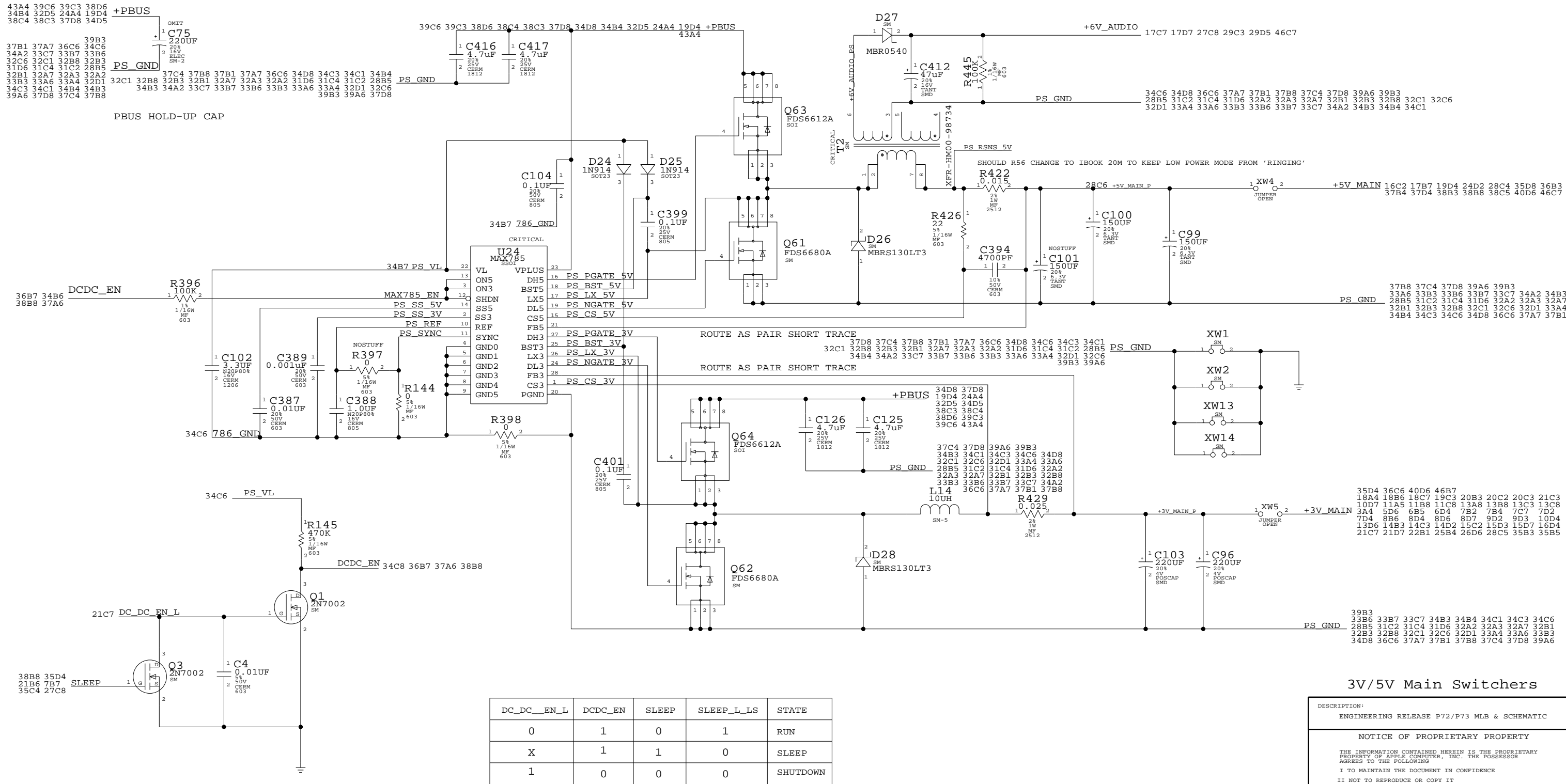
BATTERY INTERFACE




 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6130-C	ACI: C ECS:1.A
	SCALE	SMT	OF
	NONE	33	53


3V/5V Main Switchers

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
126S2228	1	ELEC 220UF/16V 20%	C75	3SBAT
126S1024	1	ELEC 100UF/35V 20%	C75	4SBAT



APPLE COMPUTER INC.

SIZE	D	DRAWING NUMBER	051-6130-C	REV.	ACT: C ECS: 1.0
SCALE	NONE	SHT	34	OF	53

 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6130-C	REV. ACI: C ECS: 1.B
	SCALE NONE	SHT 35 OF 53	

D

C

B

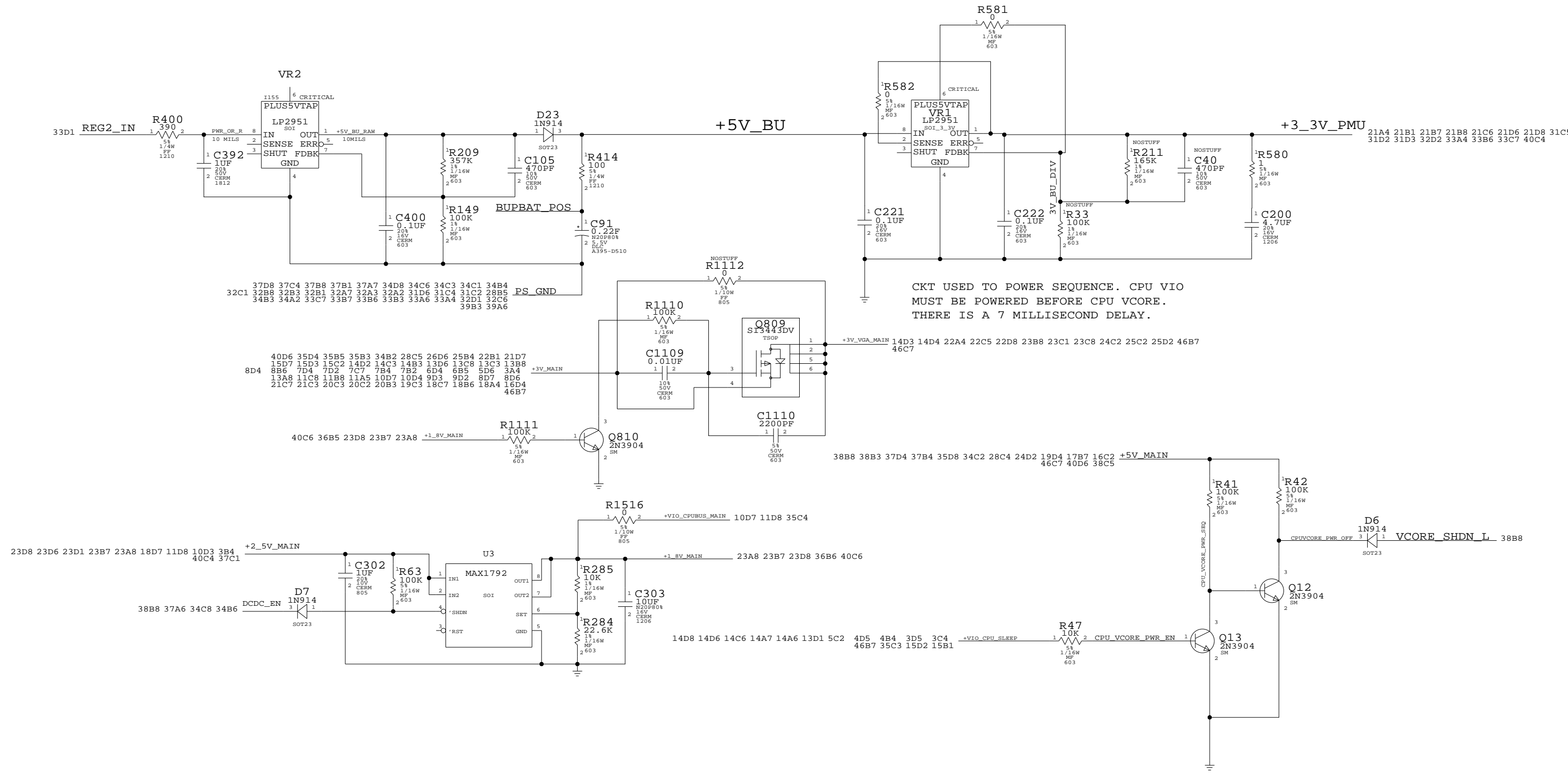
A

D

C

B

A



CKT USED TO POWER SEQUENCE. CPU VIO
MUST BE POWERED BEFORE CPU VCORE.
THERE IS A 7 MILLISECOND DELAY.

SUPER CAP CIRCUIT

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC


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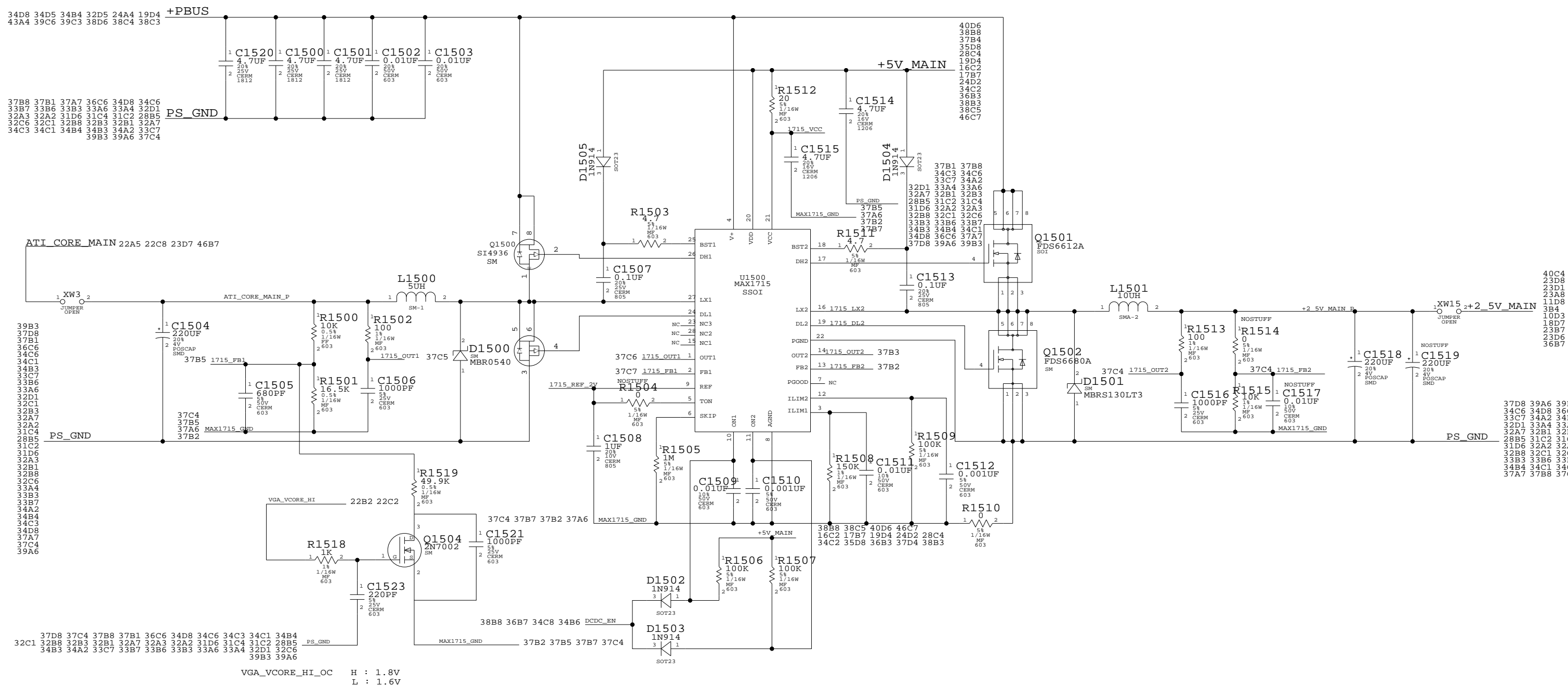
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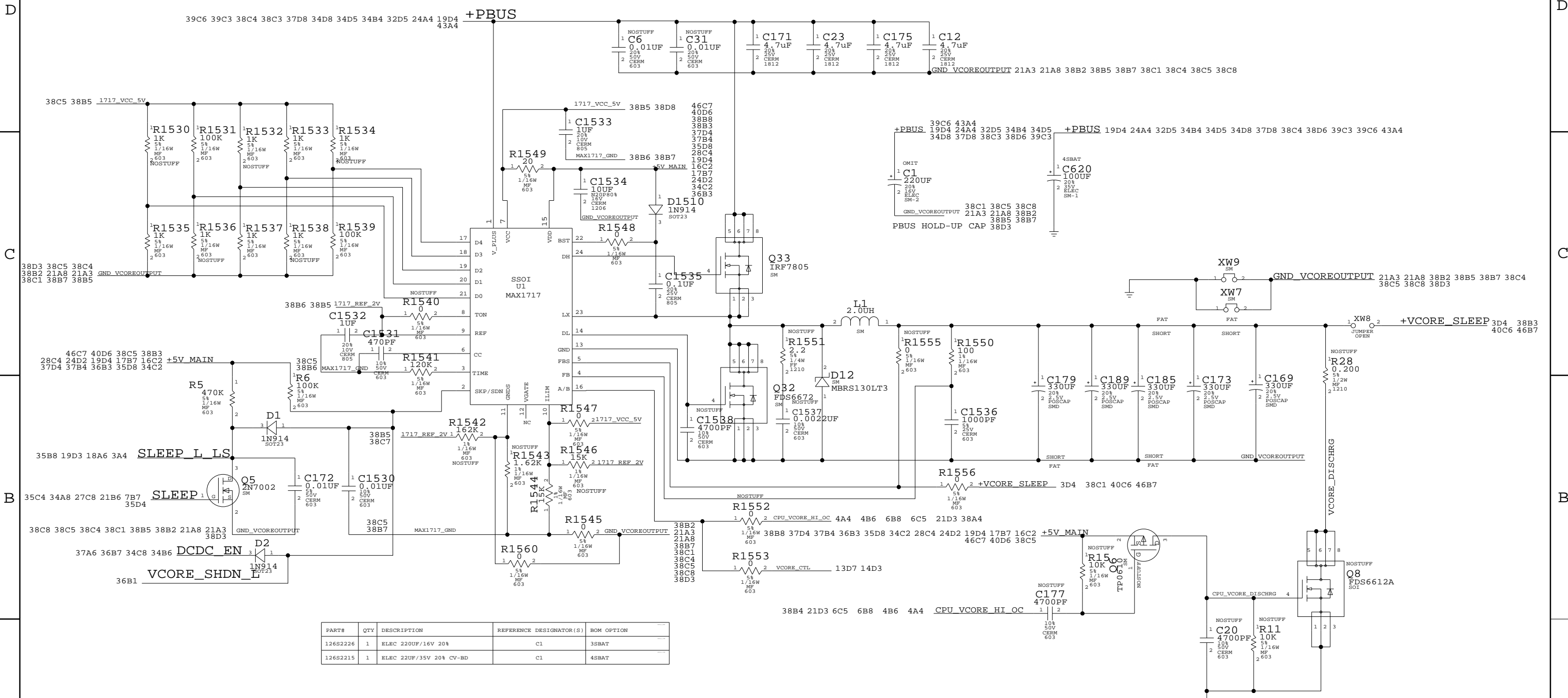
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D	051-6130-C	ACI: C ECS:1.0
SCALE	SHT	OF
NONE	37	53

CPU_VCORE(1.225/1.5V)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
126S2226	1	ELEC 220UF/16V 20%	C1	3SBAT
126S2215	1	ELEC 22UF/35V 20% CV-BD	C1	4SBAT

NOTE: SINCE ALL POWER SUPPLIES RESIDE ON THE SYSTEM BOARD JUMPERS HAVE BEEN INCORPORATED TO ALLOW ISOLATION OF THESE CIRCUITS FOR LOAD TESTING W/O THE RISK OF DAMAGE TO THE REST OF THE SYSTEM

CPU_VCORE(1.2/1.4V) & 2.5V SWITCHERS

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

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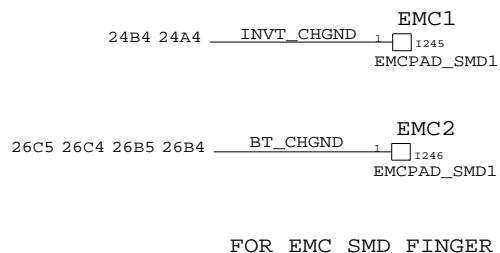
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	SCALE NONE	SHT 38 OF	53



SIZE D	DRAWING NUMBER 051-6130-C	REV. ACI: C ECS:1.0
SCALE NONE	SHT 39	OF 53

CR-411

SIG_NAME	MIN_LINE_WIDTH	VOLTAGE
+5V_MAIN		5
+3V_MAIN		3.3
		0
+2_5V_SLEEP	10	2.5
+VCORE_SLEEP	10	1.8
+3V_AVDD5_PANGAEA_MAIN	10	3.3
+3V_AVDD4_PANGAEA_MAIN	10	3.3
+3V_AVDD6_PANGAEA_MAIN	10	3.3
AGPVREF	10	
+3V_AMVDD_PANGAEA_MAIN	10	3.3
PANGAEA_TEI		0
ETH_RXD_PD		0
GBE_REFCLK		0
+3V_PHY_AVDD_MAIN		3.3
+VP_CPS		
+3V_FW_MAIN		3.3
+3V_PHY_AVDD_MAIN		3.3
+PBUS_FW_SW		
+FW_VP_FUSE_SW		
+VP_SW		
+VP_CONN_SW		
GNDRET_FW		
+5V_IO_SLEEP	20	
+5V_VGA_FUSE	20	
+1_8V_MAIN	10	1.8
+1_8V_1644_LX	10	
+1_8V_1644_FB	10	

SIG_NAME	MIN_LINE_WIDTH	VOLTAGE
+3V_SLEEP	25	3.3
+3V_VDDA3_PANGAEA_MAIN	10	3.3
+3V_VDDA3_PANGAEA_MAIN	10	3.3
+3V_VDDA3_PANGAEA_MAIN	10	3.3
VDD_USB	10	3.3
USB_PWR_A		3.3
USB_PWR_B		3.3
USB_PWR_FLT_AB		5
USB_PWR_FLT_CD		5
+3_3V_PMU	10	3.3
+3_3V_REF_PMU	10	3.3
+2_5V_ATTLEVDD_MAIN	10	2.5
+2_5V_F_A2VDDATI_MAIN	10	2.5
+2_5V_MAIN	10	2.5
+3V_AGPVDD_MAIN	10	3.3
+3V_VDDA1_PANGAEA_MAIN	10	3.3
+3V_VDDA2_PANGAEA_MAIN	10	3.3
MOBM3G1	10	0
MOBM3G2	10	0
MOBM3G3	10	0
MOBM3V1	10	2.5
MOBM3V2	10	2.5
MOBM3V3	10	2.5
TXVSSR1	10	0
PANGAEA_ACS_REF	10	0
PANGAEA_SD_REF	10	0
VREF_VDDQ	10	3.3

XWS	SHORT	OPEN
XW1	X	
XW2	X	
XW3	X	
XW4	X	
XW5	X	
XW6	X	
XW7	X	
XW8	X	
XW9	X	
XW10	X	
XW11	X	
XW12	X	
XW13	X	
XW14	X	

I/O CONNECTORS
USB SHEET 17 J7,J10
ETHERNET SHEET 18 J3
FIREWIRE SHEET 19 J5
RGB SHEET 24 J12
HEADPHONE SHEET 27 J13
DC IN SHEET 32 J20

Holes and Slots
AND EMC INFO

CONSTRAINTS -- POWER

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051-6130-C

ACI: C

ECS:1.0

NONE

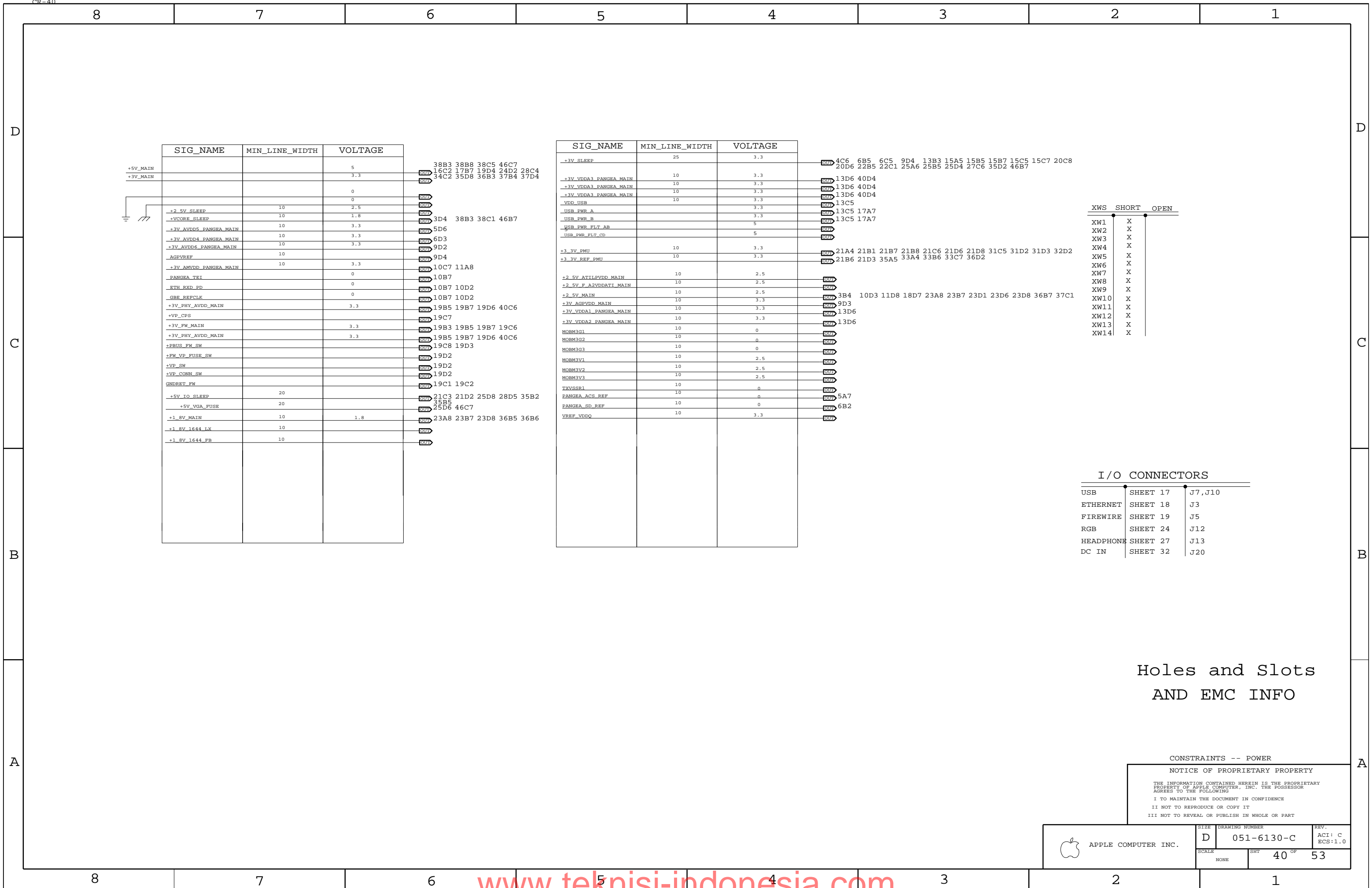
SMT

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SIG_NAME		PULSE_PARAM		MAX_VIA_COUNT		DELAY_RULE		STUB_LENGTH ECL		NET_SPACING_TYPE		NET_SCHED			
MDATA<0>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.AG1 J1.3 U23.2			
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MDATA<16>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.R1 J1.83 U24.2			
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MDATA<34>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.AC3 J1.8 U22.5			
MDATA<35>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.AC5 J1.10 U22.7			
MDATA<36>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.AC6 J1.14 U22.8			
MDATA<37>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.AC7 J1.16 U22.10			
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MDATA<40>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.AA5 J1.38 U22.42			
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MDATA<43>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.AC1 J1.44 U22.47			
MDATA<44>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.V3 J1.48 U22.48			
MDATA<45>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.V5 J1.50 U22.50			
MDATA<46>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.V6 J1.52 U22.51			
MDATA<47>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.W7 J1.54 U22.53			
MDATA<48>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.U3 J1.84 U25.2			
MDATA<49>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.U5 J1.86 U25.4			
MDATA<50>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.U6 J1.88 U25.5			
MDATA<51>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.U7 J1.90 U25.7			
MDATA<52>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.R6 J1.94 U25.8			
MDATA<53>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.R7 J1.96 U25.10			
MDATA<54>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.P5 J1.98 U25.11			
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MDATA<56>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.L6 J1.122 U25.42			
MDATA<57>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.L7 J1.124 U25.44			
MDATA<58>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.K6 J1.126 U25.45			
MDATA<59>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.K7 J1.128 U25.47			
MDATA<60>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.J3 J1.132 U25.48			
MDATA<61>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.J5 J1.134 U25.50			
MDATA<62>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.J6 J1.136 U25.51			
MDATA<63>		100		6		::1930:4400		200 TRUE		5 MIL SPACING		U1.J7 J1.138 U25.53			
SIG_NAME		PULSE_PARAM		MIN LINE WIDTH MAX_VIA_COUNT		NET_SCHED		DELAY_RULE		MAX_EXPOSED_LENGTH		STUB_LENGTH ECL		NET_SPACING_TYPE	
PANGAMCLK<0>		100		3 6				::300:500		250		100 TRUE			
PANGAMCLK<1>		100		3 6				::300:500		250		100 TRUE			
PANGAMCLK<2>		100		3 6				::300:500		250		100 TRUE			
PANGAMCLK<3>		100		3 6				::300:500		250		100 TRUE			
6D4 7C3 7D5 8D5															
6D4 7C3 7D5 8D5															
MCLK<0>		100		4 6				::1100:3500		250		100 TRUE		7C4 6D6 7A2 7A4 7C2 6D6 8B4	
MCLK<1>		100		4 6				::1100:3500		250		100 TRUE			
8C5 7D5 8C5								::1100:3500		250		100 TRUE			
MCLK<3>		100		4 6										6C5 8C5	
6D4 7C3 7D5 8C5															
6D4 7															

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AGP RELATED DOO-DAHS

CONSTRAINTS -- AGP, FIREWIRE

SIG_NAME	PULSE_PARAM / MAX_VIA_COUNT	MAX_EXPOSED_LENGTH / STUB_LENGTH	NET_SCHED	NET_SPACING_TYPE	DELAY_RULE	DELAY_RULE (THE SEQUENCE)
AGP_CLK	66 / 12	250 / 200	R213.1 U5.AG16	10 MIL SPACING	::3800:3900	5
PANGEA_AGP_CLK	66 / 3	250 / 200		10 MIL SPACING	::0225:0275	5
AGP_FB_IN	66 / 3	/ 200		10 MIL SPACING	::1325:1350	5
AGP_FB_OUT	66 / 3	/ 200		10 MIL SPACING	::0320:0335	5
AGPAD<31>	66 / 8	/ 200	U1.B11 U5.AK14	5 MIL SPACING	::3750:3980	
AGPAD<30>	66 / 8	/ 200	U1.E11 U5.AG14	5 MIL SPACING	::3750:3980	
AGPAD<29>	66 / 8	/ 200	U1.F12 U5.AG15	5 MIL SPACING	::3750:3980	
AGPAD<28>	66 / 8	/ 200	U1.C9 U5.AH14	5 MIL SPACING	::3750:3980	
AGPAD<27>	66 / 8	/ 200	U1.A9 U5.AJ15	5 MIL SPACING	::3750:3980	
AGPAD<26>	66 / 8	/ 200	U1.F11 U5.AH15	5 MIL SPACING	::3750:3980	
AGPAD<25>	66 / 8	/ 200	U1.A8 U5.AK16	5 MIL SPACING	::3750:3980	
AGPAD<24>	66 / 8	/ 200	U1.G11 U5.AK17	5 MIL SPACING	::3750:3980	
AGPAD<23>	66 / 8	/ 200	U1.B10 U5.AJ16	5 MIL SPACING	::3750:3980	
AGPAD<22>	66 / 8	/ 200	U1.A10 U5.AH18	5 MIL SPACING	::3750:3980	
AGPAD<21>	66 / 8	/ 200	U1.B9 U5.AK19	5 MIL SPACING	::3750:3980	
AGPAD<20>	66 / 8	/ 200	U1.B8 U5.AJ18	5 MIL SPACING	::3750:3980	
AGPAD<19>	66 / 8	/ 200	U1.E12 U5.AG18	5 MIL SPACING	::3750:3980	
AGPAD<18>	66 / 8	/ 200	U1.C8 U5.AJ19	5 MIL SPACING	::3750:3980	
AGPAD<17>	66 / 8	/ 200	U1.C11 U5.AH19	5 MIL SPACING	::3750:3980	
AGPAD<16>	66 / 8	/ 200	U1.A7 U5.AG19	5 MIL SPACING	::3750:3980	
AGPAD<15>	66 / 8	/ 200	U1.E14 U5.AJ22	5 MIL SPACING	::3020:3270	
AGPAD<14>	66 / 8	/ 200	U1.F14 U5.AH22	5 MIL SPACING	::3020:3270	
AGPAD<13>	66 / 8	/ 200	U1.C12 U5.AK22	5 MIL SPACING	::3020:3270	
AGPAD<12>	66 / 8	/ 200	U1.F15 U5.AG23	5 MIL SPACING	::3020:3270	
AGPAD<11>	66 / 8	/ 200	U1.C14 U5.AH23	5 MIL SPACING	::3020:3270	
AGPAD<10>	66 / 8	/ 200	U1.F13 U5.AK25	5 MIL SPACING	::3020:3270	
AGPAD<9>	66 / 8	/ 200	U1.A12 U5.AK23	5 MIL SPACING	::3020:3270	
AGPAD<8>	66 / 8	/ 200	U1.B12 U5.AH24	5 MIL SPACING	::3020:3270	
AGPAD<7>	66 / 8	/ 200	U1.B13 U5.AK27	5 MIL SPACING	::3020:3270	
AGPAD<6>	66 / 8	/ 200	U1.C15 U5.AK24	5 MIL SPACING	::3020:3270	
AGPAD<5>	66 / 8	/ 200	U1.B14 U5.AH26	5 MIL SPACING	::3020:3270	
AGPAD<4>	66 / 8	/ 200	U1.F16 U5.AG24	5 MIL SPACING	::3020:3270	
AGPAD<3>	66 / 8	/ 200	U1.A11 U5.AJ27	5 MIL SPACING	::3020:3270	
AGPAD<2>	66 / 8	/ 200	U1.A13 U5.AK26	5 MIL SPACING	::3020:3270	
AGPAD<1>	66 / 8	/ 200	U1.A14 U5.AH27	5 MIL SPACING	::3020:3270	
AGPAD<0>	66 / 8	/ 200	U1.E15 U5.AJ28	5 MIL SPACING	::3020:3270	
AGPADSTB<1>	66 / 8	/ 200	R779.2 U5.AG17	10 MIL SPACING	::0500:0550	
AGPADSTB<0>	66 / 8	/ 200	R778.2 U5.AH25	10 MIL SPACING	::0600:0650	
AGPSBA<7>	66 / 8	/ 200		5 MIL SPACING		
AGPSBA<6>	66 / 8	/ 200		5 MIL SPACING		
AGPSBA<5>	66 / 8	/ 200		5 MIL SPACING		
AGPSBA<4>	66 / 8	/ 200		5 MIL SPACING		
AGPSBA<3>	66 / 8	/ 200		5 MIL SPACING		
AGPSBA<2>	66 / 8	/ 200		5 MIL SPACING		
AGPSBA<1>	66 / 8	/ 200		5 MIL SPACING		
AGPSBA<0>	66 / 8	/ 200		5 MIL SPACING		
AGPSBSTB	66 / 5	/ 200		10 MIL SPACING	::4385:4490	
AGECBE<3>	66 / 8	/ 200	U1.F9 U5.AK18	5 MIL SPACING	::3750:3980	
AGECBE<2>	66 / 8	/ 200	U1.F9 U5.AK21	5 MIL SPACING	::3750:3980	
AGECBE<1>	66 / 8	/ 200	U1.A6 U5.AG22	5 MIL SPACING	::3020:3270	
AGECBE<0>	66 / 8	/ 200	U1.F10 U5.AJ24	5 MIL SPACING	::3020:3270	
AGPST<2>	66 / 8	/ 200	U1.A15 U5.AK12	5 MIL SPACING	::3500:4500	
AGPST<1>	66 / 8	/ 200	U1.G16 U5.AJ12	5 MIL SPACING	::3500:4500	
AGPST<0>	66 / 8	/ 200	U1.B15 U5.AG12	5 MIL SPACING	::3500:4500	
AGPPAR	66 / 8	/ 200	U1.A16 U5.AJ21	5 MIL SPACING	::3500:4500	
AGPFRAME*	66 / 8	/ 200	U1.B17 U5.AH20	5 MIL SPACING	::3500:4500	
AGPTRDY*	66 / 8	/ 200	U1.B16 U5.AK20	5 MIL SPACING	::3500:4500	
AGPIRDY*	66 / 8	/ 200	U1.C17 U5.AG20	5 MIL SPACING	::3500:4500	
PCISTOP*	66 / 8	/ 200	U1.E17 U5.AH21	5 MIL SPACING	::3500:4500	
AGPDEVSEL*	66 / 8	/ 200	U1.B7 U5.AG21	5 MIL SPACING	::3500:4500	
AGPIPE*	66 / 8	/ 200	U1.B5 U5.AG13	5 MIL SPACING	::3500:4500	
AGPRBF*	66 / 8	/ 200	U1.B6 U5.AH12	5 MIL SPACING	::3500:4500	

MIN_LINE_WIDTH

9C5 22C6

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FIREWIRE RELATED DOO-DAHS

SIG_NAME	PULSE_PARAM / MAX_VIA_COUNT	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	
FW_XI	24.576 / 2	250	200	10 MIL SPACING	
FW_XO	24.576 / 2	250	200	10 MIL SPACING	
FW_LINK_SCLK	49.152 / 4	250	200	10 MIL SPACING	
PHYSCLK	49.152 / 4	250	200	10 MIL SPACING	
FW_LINK_D<7>	49.152 / 4		200		
FW_LINK_D<6>	49.152 / 4		200		
FW_LINK_D<5>	49.152 / 4		200		
FW_LINK_D<4>	49.152 / 4		200		
FW_LINK_D<3>	49.152 / 4		200		
FW_LINK_D<2>	49.152 / 4		200		
FW_LINK_D<1>	49.152 / 4		200		
FW_LINK_D<0>	49.152 / 4		200		
FW_LINK_CNTL1	49.152 / 4		200		
FW_LINK_CNTL0	49.152 / 4		220		
FW_LINK_LREQ	49.152 / 4		200		
PHYD7	49.152 / 4		200		
PHYD6	49.152 / 4		200		
PHYD5	49.152 / 4		200		
PHYD4	49.152 / 4		200		
PHYD3	49.152 / 4		200		
PHYD2	49.152 / 4		200		
PHYD1	49.152 / 4		200		
PHYD0	49.152 / 4		200		
PHYCNTL1	49.152 / 4		200	5 MIL SPACING	
PHYCNTL0	49.152 / 4		200	5 MIL SPACING	
PHYLREQ	49.152 / 4		200	5 MIL SPACING	

FIREWIRE DIFFERENTIAL THINGIES

SIG_NAME	PULSE_PARAM / MAX_VIA_COUNT	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	ECL	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PHYTPA0T	400 / 2	250		TRUE		PHYTPA0
PHYTPA0C	400 / 2	250		TRUE		PHYTPA0
PHYTPB0T	400 / 2	250		TRUE		PHYTPB0
PHYTPB0C	400 / 2	250		TRUE		PHYTPB0
PHYTPA0T_FL	400 / 2	250		TRUE		PHYTPA0_FL
PHYTPA0C_FL	400 / 2	250		TRUE		PHYTPA0_FL
PHYTPB0T_FL	400 / 2	250		TRUE		PHYTPB0_FL
PHYTPB0C_FL	400 / 2	250		TRUE		PHYTPB0_FL

CONSTRAINTS -- AGP, FIREWIRE

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ECS:1.0

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MLB STACKUP

CPU ROUTES ARE ? OHMS?
AGP ROUTES ARE 5 MILS OHMS?
RAM ROUTES ARE ? OHMS?

SIZE D	DRAWING NUMBER 051-6130-C	REV. ACI: C ECS:1.0
SCALE NONE	SHT 46	OF 53

8	7	6	5	4	3	2	1
D	REVISION HISTORY (1)						
	SAHARA QUAL PCB(REV:0.0)						
	1) CHANGE CPU FROM SIDEWINDER TO SAHARA 2) CHANGE VGA FROM ATI-M3 TO ATI-M6 3) CHANGE AUDIO FROM TUMBLER TO SNAPPER						
C	PROTO (REV:0.1)						
	1) ACCORDING RADAR#2773492 - UPDATES TO THE P72 SCHEMATICS 2) ACCORDING RADAR#2774277 - P72 M6 SCHEMATICS FIXES FOR PROTO2 A) UNSTUFF R902,R903,R905 B) CHANGE R906 TO 100K AND PULL UP TO VDDC C) STUFF R914,R916 FOR M6 16MB VERSION D) ADD R1116(0OHM) BETWEEN C954 AND C955 E) UNSTUFF R395 AND Q56 3) ACCORDING RADAR#2775061 - CHANGE P72 TO HARDWARE CHARGING 4) ACCORDING RADAR#2777820 - NEW AVC CABLE CONNECTIONS A) ADD U210(74LVC1G125),F100,Q210,Q211,C1210,R957,R958,R959 FOR NEW AVC CONNCETOR. 5) ACCORDING RADAR#2780508 - CHANGE TO THE AUDIO POWER DOWN CIRCUIT A) REMOVE R462,R599,R600,R601,R602,R603,C638,Q86,Q87 B) CONNECT U300/PIN8 TO DGND C) CONNECT U300/PIN6 TO IO_RESET_L D) CHANGE U4/PIN AA33 NAME FROM AUDIO_HW_RESET_L TO PAN_GPIO1 E) ADD 10K PULLUP FOR PAN_GPIO1 6) ACCORDING RADAR#2779003 - ADD A BOM OPTION TO PREPARE FOR SAHARA DD2.0 7) ACCORDING RADAR#2780490 - NEW FAN SPEED CONTROL CIRCUIT A) ADD U1200(ADM1030) AND Q1000 FOR NEW FAN CONTROL CIRCUIT 8) ACCORDING RADAR#2782007 - DASH MODEM PERFORMANCEIMPACTED BY VCORE SWITCHER A) DISCONNECT ZH2 FROM GND 9) ACCORDING RADAR#2782669 - ADD OPTIONAL CONTROL FOR VCORE VLOTAGE A) CHANGE U4/PIN AA33 NET NAME FROM PAN_GPIO1 TO VCORE_CTL B) REMOVE THE NET NAME "CPU_VCORE_HI_OC" FROM U1/PIN16 C) ADD R1552 BETWEEN U1/PIN16 AND THE NET "CPU_VCORE_HI_OC" D) ADD R1553(NOSTUFF) BETWEEN U1/PIN16 AND NET "VCORE_CTL" 10) ACCORDING RADAR#2782721 - ADDITIONAL M6 CHANGES FOR OK TO FAB A) ADD R954 FOR VGA CORE HI_OC SIGNAL PULLUP B) CHANGE Q1504/PIN2 CONNECTION FROM PS_GND TO MAX1715_GND C) CHANGE THE NET NAME FROM VGA_VCORE_HI_OC TO VGA_VCORE_HI 11) ACCORDING RADAR#2782641 - EXTERNAL VIDEO SCHEMATICS CHANGE A) REMOVE R394,R393,R395,Q56,R392,C905 B) CHANGE R935,R936,R937 CONNECTION FROM U200/PIN AF22,AF23,AF24 TO U200/PIN AF14,AF15,AF16 C) REMOVE COMPVSS SIGNAL AND L36 12) ACCORDING RADAR#2784789 - PROTO BUILD BOM CHANGES A) STUFF R803(113S1102),R805(113S1473,R820(113S1000),R1110,R1111,C1109,C1110,Q809,Q810 B) UNSTUFF R1115,R1112,Q211 C) CHANGE R539 TO 3.16K,1% (110S3163)						
	B	EVT (REV:0.2)					
1) ACCORDING RADAR#2798007 - ADD AUDIO/CONTROL CONNECTOR A) USE J900(NEW FOXCONN AUDIO JACK) TO REPLACE J13 B) ADD CONTROL CIRCUITS FOR I-POD 2) ACCORDING RADAR#2794270 - SCHEMATICS CHANGE-NEW BLUETOOTH CONN. A) USE 4PIN J100 CONN TO REPLACE J100(6PIN) B) CHANGE THE USB-D CIRCUITS FOR BLUETOOTH MODULE. 3) ACCORDING RADAR#2805677 - CHANGES FROM EVT LAYOUT REVIEW A) ADD R1300 BETWEEN J200-1 AND PAN_XIB B) ADD BYPASS CAP C1100 NEAR U802 ON +3V_CLKGEN_SLEEP C) MOVE RESISTORS R963,R964 AND R965 NEAR PANGEA D) CHANGE C803,C804 AND C805 FORM 1.0U TO 10.0U WITH 0805 PACKAGE E) ADD 4 MORE VIAS WHERE +3VCORE_SLEEP OF C800,C801,C836 F) ADD AN EXTRA VIA ON PIN9 OF U32 TO GROUND G) MAKE THE TRACE FROM PIN2 OF D31 GO FIRST TO PIN1 OF C156,THEN TO PIN2 OF R1557 H) MOVE R1555 CLOSER TO U1 AND L1 4) ACCORDING RADAR#2805288 - CHANGE TO OVERTEMP CIRCUIT A) CHANGE R1206 FORM 39K TO 27K 5) ACCORDING RADAR#2805242 - ADD RESISTOR TO SCC RTS SIGNAL FOR TESTING PURPOSES A) ADD R967 BETWEEN PIN1 OF U210 AND SCC_RTSA* B) NAMED SLINK_TX_ENABLE_L ON U210 PIN1 6) ACCORDING RADAR#2794331 - REMOVE BLEED CIRCUIT FOR VCORE RAIL A) NOSTUFF C177,R15,Q6,C20,R11,Q8							
A		7) ACCORDING RADAR#2804787 - SCHEMATIC CHANGE-MOVE FAN TO SLEEP RAIL A) USE J900(NEW FOXCONN AUDIO JACK) TO REPLACE J13 8) ACCORDING RADAR#2801304 - RETURN JOLLY ROGER OPTION A) CONNECT SCC_RTSA* TO PIN6 OF J2 THROUGH A NOSTUFF 0 OHM RESISTOR B) CONNECT SCC_RXDA TO PIN9 OF J2 THROUGH A NOSTUFF 0 OHM RESISTOR C) CONNECT SCC_TXDA* TO PIN12 OF J2 THROUGH A NOSTUFF 0 OHM RESISTOR D) CONNECT SCC_DTRA TO PIN8 OF J2 E) CONNECT SCC_TRXCA TO PIN14 OF J2 9) ACCORDING RADAR#2804786 - REMOVE CPU_VOCRE_LO_OC CIRCUIT A) REMOVE R832 AND Q808 10) ACCORDING RADAR#2803484 - ADD SLOW_CHRG AND FAST_CHRG BOM OPTION A) ADD TWO ROW OF BOM OPTION FOR - SLOW_CHRG FOR P72, FAST_CHRG FOR P73 B) REMOVE THE HWCHG BOM FROM R539 AND ADD THE OMIT LABEL C) ADD A BOM OPTION FOR R539 - SLOW_CHRG 3.16K AND FAST_CHRG 2.61K 11) ACCORDING RADAR#2792009 - REMOVE UNUSED SCC LINES FOR MODEM A) REMOVE NETS SCC_DTRA* AND SCC_TRXCA B) KEEP THE PULLDOWN RESISTORS ON SCC_GPIOA* AND SCC_TRXCA 12) ACCORDING RADAR#2800865 - I CAN'T CHARGE IPOD WHILE IB00K IS SLEEPING A) ADD A 10BQ040 ,CATHODE CONNECT TO +FW_VP_FUSE_SW AND ANODE TO +28V_PWRBUS_SW 13) ACCORDING RADAR#2802944 - ATI SUGGESTION FOR AGP SUSPEND A) ADD A 0 OHM RESISTOR R966 BETWEEN AGP_SUS_STAT_L_PU AND AGPSTOP* 14) ACCORDING RADAR#2803479 - CHANGE SOME TANTALUM AUDIO CAPS TO CERAMIC A) CHANGE C607,C608 AND C391 FROM 1.0U TANT(127S1001) TO 1.0U CERMIC (132S1061) 15) ACCORDING RADAR#2803487 - MODIFICATION TO BATTERY CHARGING CIRCUIT A) ADD A 0 OHM RESISTOR SERIES BETWEEN PIN12 OF U32 AND PIN2 OF D31 B) ADD A NOSTUFF 0.01U 003 CAP BETWEEN PIN4 OF Q73 AND PS_GND 16) ACCORDING RADAR#2794253 - TBEN CIRCUIT-CHANGE D FLIP FLOPS TO JK A) REPLACE THE DIVIDEBY THREE CIRCUIT WITH A DUAL J-K FLIP FLOP 74LVC109 17) ACCORDING RADAR#2800233 - CHANGE POWER SUPPLY FOR INTERNAL M6 DDR MEMORY A) CHANGE THE VDDM OF M6 TO 2.5V. SO, UNSTUFF R949 AND STUFF R950 18) ACCORDING RADAR#2794264 - AC CONNECTOR WAKE FROM SLEEP CIRCUIT CAHNGE A) MOVE F100 FROM PAGE 25 TO PAGE 28 B) REMOVE TP210 AND TP211 19) ACCORDING RADAR#2794755 - HSYNC AND VSYNC NEED TO BE MOVED TO DAC2 A) MOVE ATI_VSYNC FROM PIN AE23 TO PIN AF13 B) MOVE ATI_HSYNC FROM PIN AE24 TO PIN AE14 20) ACCORDING RADAR#2795893 - VGA_VCORE_HI NEEDS TO BE HIGH AT POWERON A) CHANGE R956 TO 10K AND CONNECT TO +3V_MAIN 21) ACCORDING RADAR#2795903 - UNSTUFFED COMPONENTS ON SCHEMATICS A) UNSTUFF R1112 AND STUFF R1111,R1110,C1109,C1110,Q810 AND Q809 22) ACCORDING RADAR#2797834 - REMOVE PMU RESET BUTTON A) NOSTUFF S4 23) ACCORDING RADAR#2754201- LENGTH CONSTRAINTS FOR CPU BUS SIGNALS A) CHANGE THE CONSTRAINTS OF CPU BUS TO 2500:3500 AND THE MAX COUT OF VIA TO 5 24) ACCORDING RADAR#2794312 - FAN CIRCUITRY CHANGE A) CHANGE THE NAME OF THERM* TO THERM_OD* B) CHANGE R1206 TO 39K 25) ACCORDING RADAR#2794262- INVESTIGATE M6 PLL POWER RAIL ARRANGEMENT A) UNSTUFF R951 AND CONNECT +1_8V_PVDD_MAIN TO +1_8V_LVDDR_MAIN 26) ACCORDING RADAR#2794249 - NEW SPREAD SPECTRUM PART A) CHANGE THE SPREAD SPECTRUM CHIP FROM IMI C9531 TO CYPRESS CY28507 B) ADD 2 RESISTORS - ONE BETWEEN PMU_IIC_CLK AND +3_3V_PMU ANOTHER IS PMU_IIC_DAT AND +3_3V_PMU 27) ACCORDING RADAR#2779003 - ADD A BOM OPTION TO PREPARE FOR SAHARA DD2.0 A) SET DD1X BOM OPTION FOR P72/P73 AND CHANGE THE BOM OPTION OF Q800,Q801,R804,R805 TO DD1X 28) ACCORDING RADAR#2780490 - NEW FAN SPEED CONTROL CIRCUIT A) ADD A NEW FAN CONTROL CIRCUIT ADM1030 TO REPLACE THE TWO THERMOSTATS 29) ACCORDING RADAR#2791511 - ADD PMU RESET FROM KEYBOARD CIRCUIT A) ADD RESET FUNCTION BY PRESSING THE SHIFT-CONTROL-FN-POWER KEY TO REPLACE RESET SWITCH 30) ACCORDING RADAR#2794257 - CHANGE NAME OF AGPREF_PD A) CHANGE THE NAME OF AGPREF_PD TO AGPREF_PU 31) ACCORDING RADAR#2794329 - REMOVE BLEED CIRCUIT FOR ATI_CORE_MAIN A) REMOVE THE CURRENT BLEED CIRCUIT FOR ATI_CORE_MAIN IN THE BOTTOM LEFT CORNER ON PAGE 37					
	DESCRIPTION: ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC						
	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART						
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REVISION HISTORY (2)

32) ACCORDING RADAR#2791719 - SCHEMATIC CHANGE - REMOVE R1115
A) REMOVE R1115 BECAUSE SLEEP_L_LS IS ALREADY PULLED UP TO 5V RAIL

33) ACCORDING RADAR#2792071 - REMOVE UNUSED RGB SIGNALS ON PAGE 22
A) REMOVE THE UNUSED RGB SINGALS ON PAGE 22 (PIN AF22,AF23,AF24 ON M6) AND ADD NC FOR THEM

34) ACCORDING RADAR#2792085 - REMOVE OLD HP_DETECT SIGNALS ON PAGE 22
A) REMOVE THE COMPVID_HP_TEST AND COMPVID_HP_DETECT FROM PAGE 22 (AC20 AND AD20 ON M6)

DVT (REV:0.3)

1) ACCORDING RADAR#2843372 - ADD BACK FIREWIRE DIODE
A) STUFF D1506

2) ACCORDING RADAR#2823008 - P72 EVT UNITS PLUG IN A BUS POWERED YANO FW HARD DRIVE - SCREEN GOES DARK. POWER PROBLEM
A) CHANGE THE NET OF D1506 PIN1 FROM +28V_PWRBUS_SW TO CHRГ_OUT AND NOSTUFF D1506
B) CHANGE C160 FROM 0.01UF TO 0.1UF

3) ACCORDING RADAR#2838736 - SCHEMATIC CHANGE - 700 MHZ AND 1.5V
A) CHANGE BOM TABLE OF CPU FROM 750MHZ TO 700MHZ
B) REMOVE THE BOM OPTION ON R825
C) CHANGE 600MHZ CPU VCORE TO 1.5V

4) ACCORDING RADAR#2840812 - CHANGE ALL MCLK LINES TO USE 0 OHM SEIES TERMINATION RESISTORS
A) CHANGE R841,R843,R847 TO 0 OHM

5) ACCORDING RADAR#2831933 - P72 PLL RANGE CONFIGURATIONS
A) ALL CONFIGS SHOULD NOW HAVE THE "MID" PLL RANGE OPTIONS (NO POWERSTEP)
B) ADD "MID OR HIGH RANGE NO PWRSTEP" AND LOW OR MID PLL RANGE" ROW FOR P72 GOOD CONFIG
C) REMOVE "LOW PLL RANGE" ROW UNDER THE P72 CONFIGURATION

6) ACCORDING RADAR#2830139 - P72 IMPLEMENT POWERPLAY ON M6 ON P72
A) CHANGE C1505 TO 680P AND ADD C1521 1000P

7) ACCORDING RADAR#2831140 - P72 SCHEMAITC REVIEW ACTION ITEMS

8) ACCORDING RADAR#2824938 - REQUIRED WAKEUP PULSE ON P72 HEADPHONE JACK TAKES TOO LONG (H/W)
A) CHANGE C1210 WITH 0.047UF CAP AND PACKAGE FROM 0805 TO 0603

9) ACCORDING RADAR#2829465 - AUDIO FIX - Q900
A) PIN 2 AND 3 OF Q900 ARE REVERSED. PIN2 SHOULD CONNECT TO GROUND.

10) ACCORDING RADAR#2820867 - TBEN DIVIDE-BY-THREE SCHEMATIC REPAIR
A) CHANGE NET OF U802 PIN1 AND PIN15 FORM +3V_CLKGEN_SLEEP TO CPU_VCORE_HI_OC

11) ACCORDING RADAR#2825538 - KEYBOARD CHORD RESET OF PMU BOOTS
A) CHANGE NET OF U800 PIN5 FROM FN_KEY_L TO OPTION_KEY_L
B) NOSTUFF R19
C) CHANGE R1554 FROM 1K(113S1103) TO 10K(113S1104)

12) ACCORDING RADAR#2828251 - PMU IIC PULLUPS WRONG AT EVT
A) ADD R1120 10K RESISTOR BETWEEN +3V_SLEEP AND THE SIGNAL PMU_IIC_DAT
B) ADD R1121 10K RESISTOR BETWEEN +3V_SLEEP AND THE SIGNAL PMU_IIC_CLK
C) CHANGE THE VOLTAGE ON R1118-2 FROM +3_3V_PMU TO +3V_CLKGEN_SLEEP
D) CHANGE THE VOLTAGE ON R1119-2 FROM +3_3V_PMU TO +3V_CLKGEN_SLEEP

13) ACCORDING RADAR#2829528 - UPDATE NO PWRSTEP BOM OPTION FOR NEW PLL RANGE BITS
A) ADD R1122 10K (BETWEEN Q806 PIN2 AND PIN3) WITH "MID OR HIGH RANGE NO PWRSTEP"
B) ADD R1123 4.7K (BETWEEN Q807 PIN2 AND PIN3) WITH "HIGH PLL RANGE NO PWRSTEP"
C) CHANGE Q806 BOM OPTION TO "MID OR HIGH RANGE PWRSTEP"
D) CHANGE Q807 BOM OPTION TO "HIGH PLL RANGE PWRSTEP"
E) DELETE TWO ROWS ON PAGE 1 "MID RANGE PLL" AND "MID OR HIGH RANGE PLL"
F) ADD 4 ROWS ON PAGE 1 - "MID OR HIGH RANGE NO PWRSTEP", "HIGH PLL NO PWRSTEP", "MID OR HIGH RANGE PWRSTEP", "HIGH PLL RANGE PWRSTEP"

14) ACCORDING RADAR#2830159 - FAST CHARGE FOR ALL SYSTEM CONFIGS
A) CHANGE ALL SYSTEM CONFIGS TO USE THE FAST_CHRG OPTION ON PAGE 1

15) ACCORDING RADAR#2841691 - SERIAL LINE REMAINSAT INTERMEDIATE LEVEL
A) CHANGE R959 FORM 100K(113S1105) TO 470K (113S1475)
B) CHANGE C1210 FROM 0.047UF (132S4743) TO 0.01UF (132S1045)

DVT2 (REV:0.4)

1) ACCORDING RADAR#2855154 - SNAPPER AUDIO CHIP NEEDS SEPARATE RESET
A) ADD Q901,Q902 (2N7002), AND R1031 (100K,5%)
B) CHANGE NET NAME OF U300 PIN6 FROM IO_RESET_L TO TAS_RESET_L

2) ACCORDING RADAR#2856224 - SCHEMATIC CHANGE - ARTRY PULL UP
A) DISCONNECT ARTRY* FROM RP101
B) PULL UP ARTRY* WITH 1K RESISTOR (R1032) TO +VIO_CPU_SLEEP

3) ACCORDING RADAR#2856231 - MORE BYPASS CAPACITORS ON SAHARA
A) ADD C980,C981(10U 0805) FOR +VCORE_SLEEP

4) ACCORDING RADAR#2862722 - INCREASE BANDWIDTH OF MICROPHONE AMPLIFIER
A) CHANGE C1017 FROM 0.022UF TO 0.047UF
B) CHANGE C1021 FROM 150P TO 47P
C) CHANGE C1022 FROM 0.047UF TO 0.1UF
D) CHANGE R1019 FROM 36K TO 10K

5) ACCORDING RADAR#2831587 - P72 EVT : POP HEARD WHEN PLUG HEADPHONES INTO ANALOG LINE OUT
A) CHANGE R139 FROM 100K TO 470K

6) ACCORDING RADAR#2862391 - CHANGE NAME OF BOM OPTION
A) CHANGE R1123 BOM OPTION TO "HIGH_PLL_RANGE_NO_PWRSTEP"
B) CHANGE PAGE 1 BOM TABEL FROM "HIGH_PLL_RANGE_NO_PWRSTEP" TO "HIGH_PLL_RANGE_NO_PWRSTEP"

7) ACCORDING RADAR#2865479 - CHANGE CPU VCORE SETTING (LOW SETTING AND VOLTAGE POSITIONING)
A) CHANGE R1531 FROM 1K TO 100K FOR P72 GOOD CONFIGURATION
B) CHANGE R1535 FROM 100K TO 1K
C) DELETE R1542 AND R1543
D) ADD A 0 OHM RESISTOR R1560

PVT (REV: A)

1) ACCORDING RADAR#2868519 - SOUND LEVEL RESETS TO LOW - UPDATE FOR PVT
B) ADD A NAND GATE 74LVC1G32 FOR AUDIO RESET CIRCUIT

2) ACCORDING RADAR#2874422 - FIREWIRE DEAD ON P25 AND P92 DVT
A) ADD TWO QUAD DIODE FOR PHYTPA0T,PHYTPA0C,PHYTPB0T,PHYTPB0C

3) ACCORDING RADAR#2878614 - P72/P73 POPS FROM INTERNAL SPEAKERS POST AUDIO REWORK
A) NOSTUFF D100 AND D101
B) CHANGE C1026 AND C1027 FROM 0.047UF TO 0.1UF

4) ACCORDING RADAR#2882917 - FIREWIRE AND BATTERY CHARGING PROTECTION
A) STUFF DZ8 AND DZ9
B) CHANGE VALUE OF C467 TO 0.1UF

PVT (REV: A)

1) ACCORDING RADAR#2890158 - P72 DEPLETED BATTERY MAY NOT CHARGE IN SYSTEM
A) CHANGE R518 AND R538 FROM 100K TO 93.1K

PVT2 (REV: A)

1) ACCORDING RADAR#2910360 - MATCH P72 SPEAKER AMP TO P92
A) CHANGE C397 AND C402 FROM 0.01UF(132S1045) TO 0.047UF(132S4743)
B) CHANGE R424 AND R431 FROM 27K(113S1274) TO 20.5K(110S2054)
C) CHANGE R428 AND R423 FROM 47K(113S1474) TO 36K(113S1364)

2) ACCORDING RADAR#2917330 - ADD BOOTBANGER BOARD TO P72/73
A) ADD OASIS AND MIRAGE OPTIONS TO THE BOM OPTION TABLE AT PAGE 1
B) CHANGE THE BOM OPTION OF J19 FROM NONPRODUCTION TO OMIT AT PAGE 15
C) ADD OMIT BOM OPTION TO R1531 AND R1535 AT PAGE 38.

RAMP (REV: B)

1) ACCORDING RADAR#2917330 - ADD BOOTBANGER BOARD TO P72/P73
A) PAGE 38: CHANGE CPU VCORE SETTING TO 1.2V/1.5V
B) PAGE 14: ADD MIRAGE BOMOPTION TO R268
C) PAGE 15: ADD MIRAGE BOMOPTION TO R274

2) ACCORDING RADAR#2933296 - DIFFERENT CPU ACI P/N AND UPDATE SCH VERSION
A) PAGE 1 : ADD OASIS AND MIRAGE BOMOPTIONS FOR P72/P73
B) PAGE 3 : ADD MIRAGE CPU ACI P/N
C) CHANGE SCHEMATICS VERSION TO B

3) ACCORDING RADAR#2933252 - CHNAGE THE FAN FET TO A STRONGER PART
A) PAGE 35: CHANGE Q1001 FROM 2N7002 TO SI2302DS(372S0027)

RAMP (REV: C)

1) ACCORDING RADAR#2942313 - MORE POST-RAMP SCHEMATIC MODIFICATIONS
A) PAGE 19: STUFF FIREWIRE PROTECTION DIODES DZ8 AND DZ9
B) PAGE 16: CHANGE J2 ACI P/N TO 516S0002
C) UPDATE SCHEMATICS VERSION TO REV.C

2) ACCORDING RADAR#2945017 - F3 BOOTROM
A) PAGE 20: CHANGE BOOTROM ACI P/N TO 341S1036

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REVISION HISTORY (2)

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

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